

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU HYPER TRANSPORT
05	CPU DDRIII MEMORY
06	CPU CONTROL
07	CPU POWER & GND
08	DDRIII CHANNEL A
09	DDRIII CHANNEL B
10	RS880 HT-LINK I/F
11	RS880 PCIE I/F
12	RS880 SYSTEM I/F
13	RS880 STRAP ,SPMEM
14	RS880 POWER & GND
15	ICS9LPRS477
16	ATI SB710 PCIE/PCI/CPU/LPC
17	ATI SB710 ACPI/USB/GPIO/AUDIO
18	ATI SB710 SATA/SPI/IDE/HWM
19	ATI SB710 POWER & GND
20	PCI EXPRESS x16 ,x1
21	PCI SLOT 1, 2
22	RGB Connector
23	IDE ,FDD ,HDMI ,DVI Connector
24	COM/LPT/F_USB
25	ALC889A

[illegible]

P-Code: U97028-0

Circuit or PCB layout change for next version

GIGABYTE™

Title

BOM & PCB HISTORY

Size	Document Number
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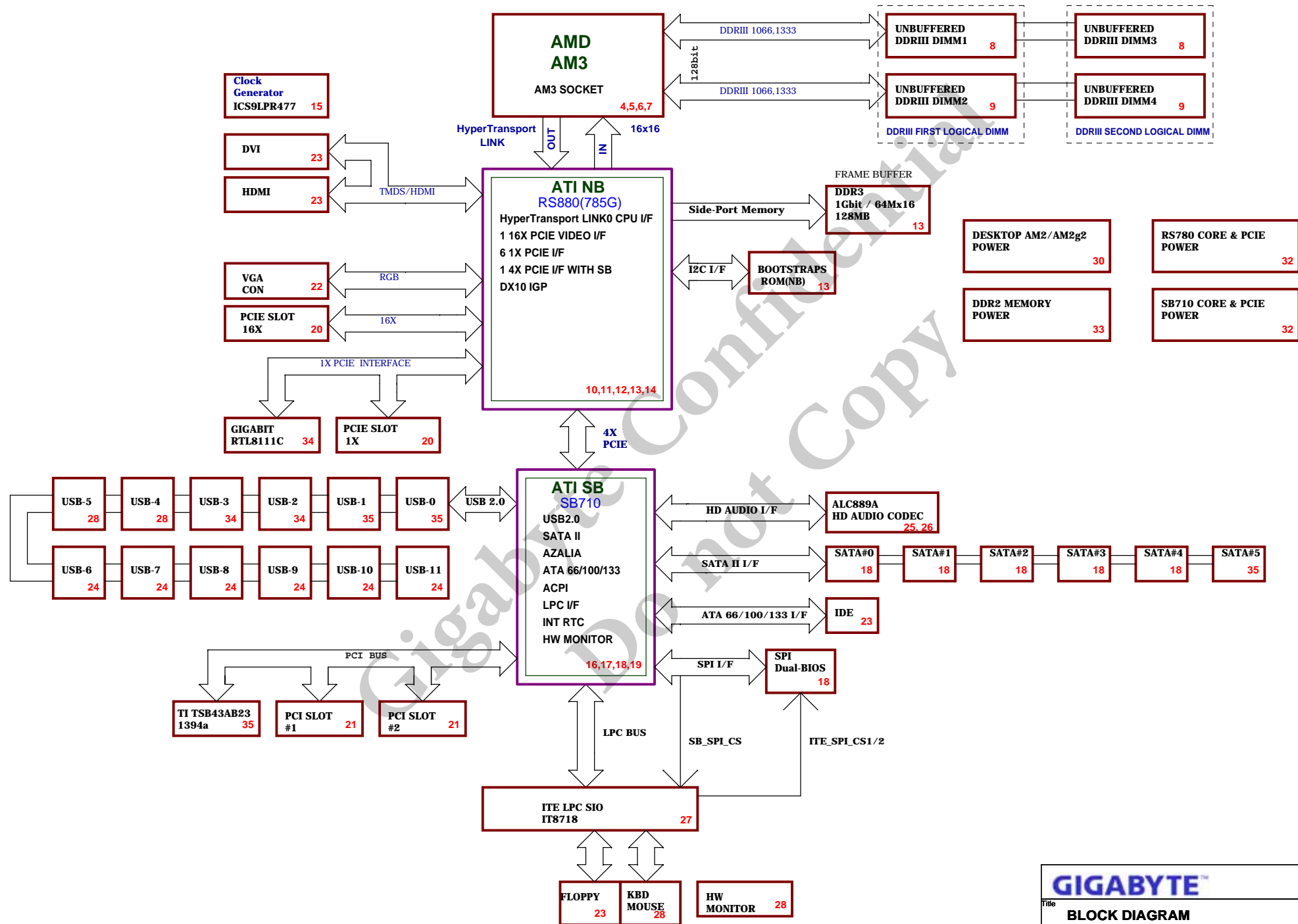
GA-MA785GMT-UD2H

Rev
1.01

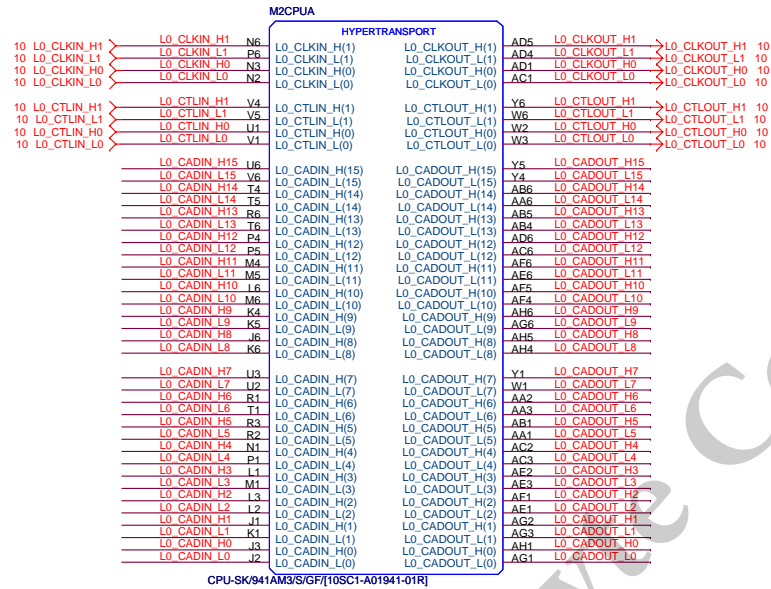
Date: Wednesday, June 17, 2009

Sheet 2 of 35

RS880 CUSTOMER DESKTOP REFERENCE DESIGN



L0_CADIN_L[0..15] < L0_CADIN_L[0..15] 10
 L0_CADIN_H[0..15] < L0_CADIN_H[0..15] 10
 L0_CADOUT_L[0..15] < L0_CADOUT_L[0..15] 10
 L0_CADOUT_H[0..15] < L0_CADOUT_H[0..15] 10

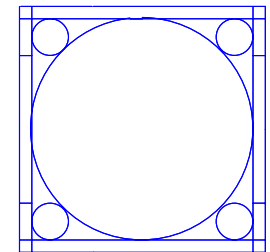


CPU_VDD_RUN = VCORE
 CPU_VDDA_RUN = VDDA25
 VLDT_RUN = VCC12_HT
 CPU_VDDIO_SUS = DDR15V
 CPU_VDDR = CPU_VDDR12

VLDT_A = VCC12_HT
 VLDT_B = HT12B

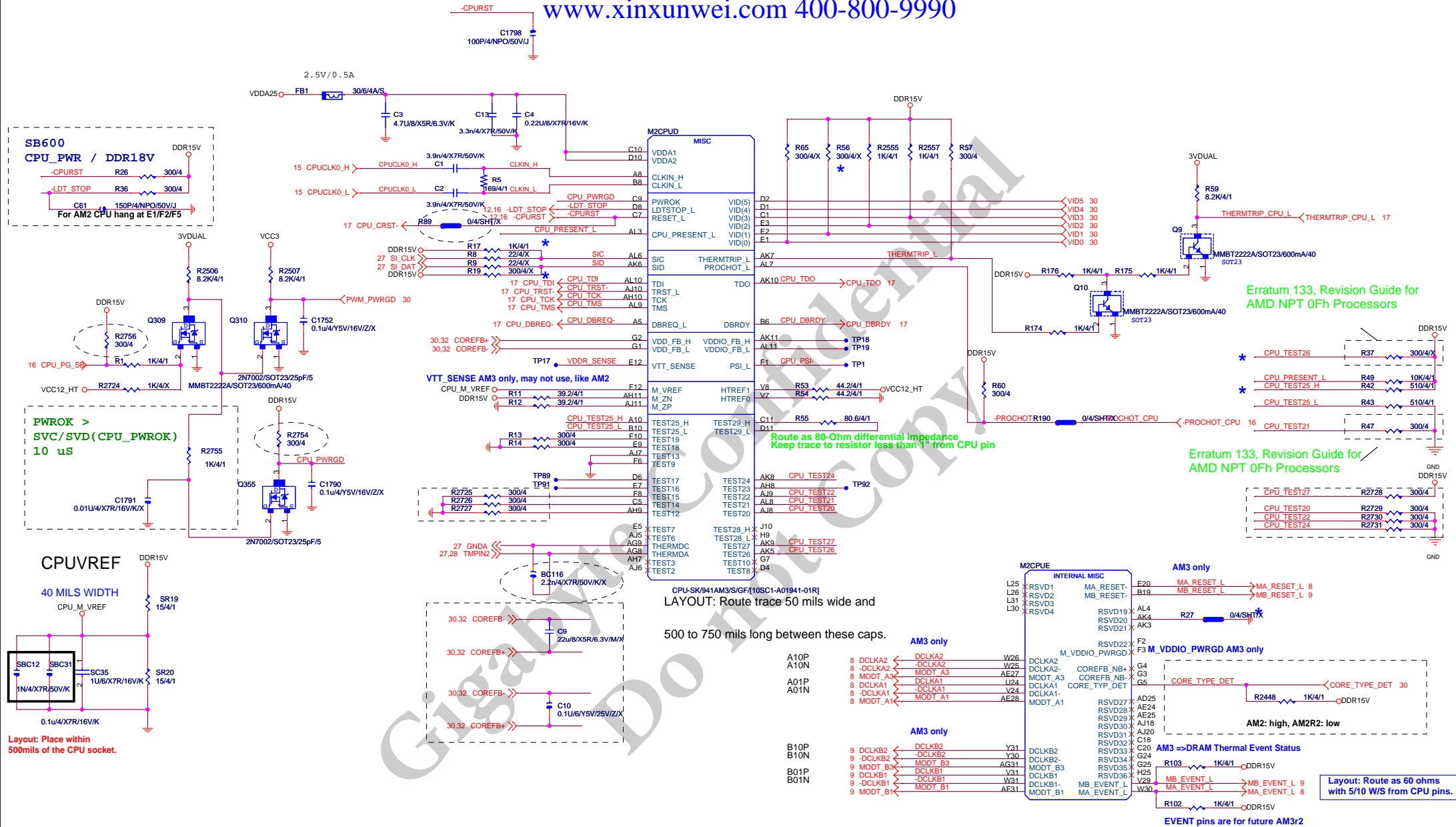
SOCKET_M2

AM2RM/PP/BU/PB/[12KRC-04K812-01R]

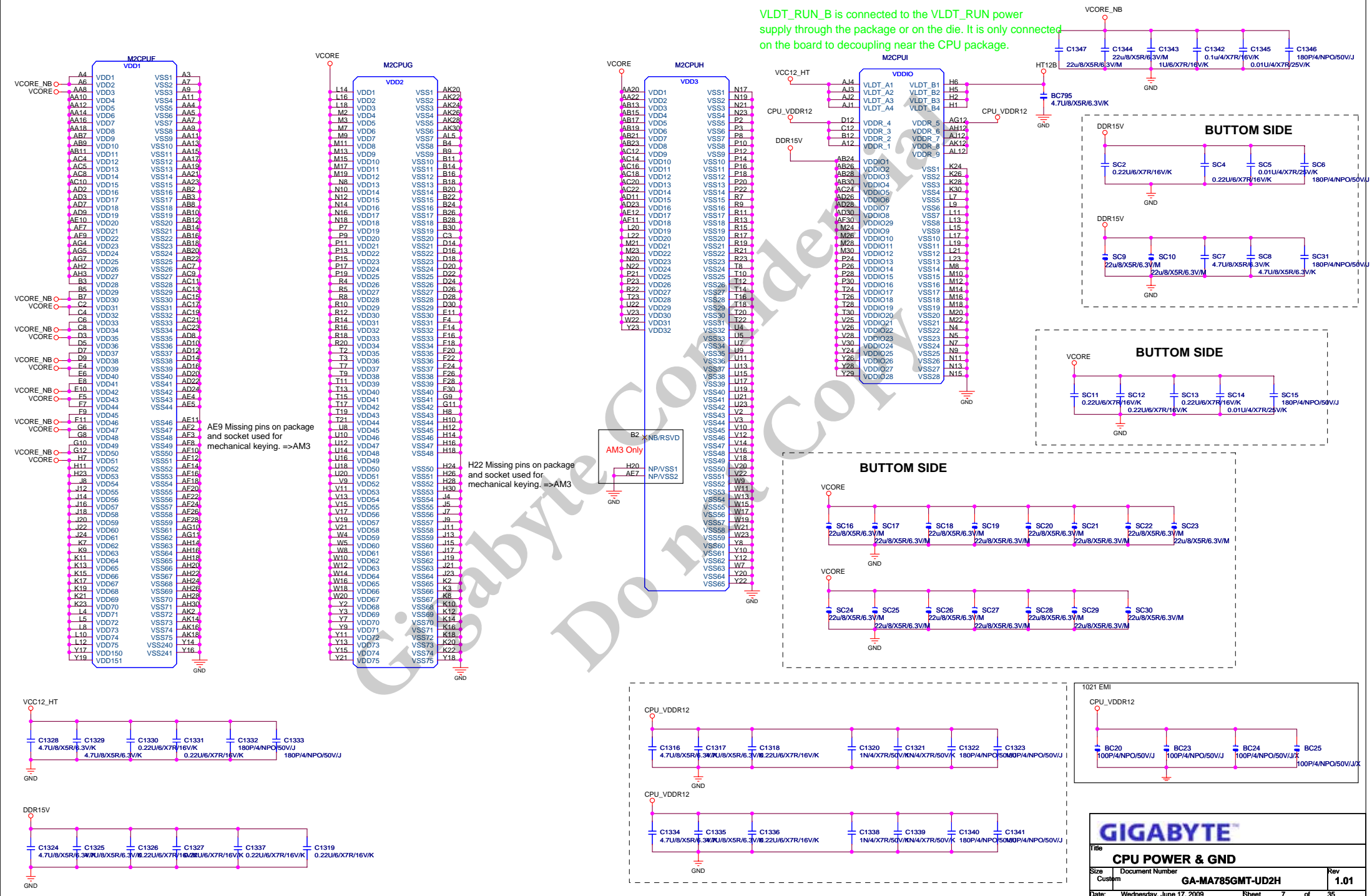


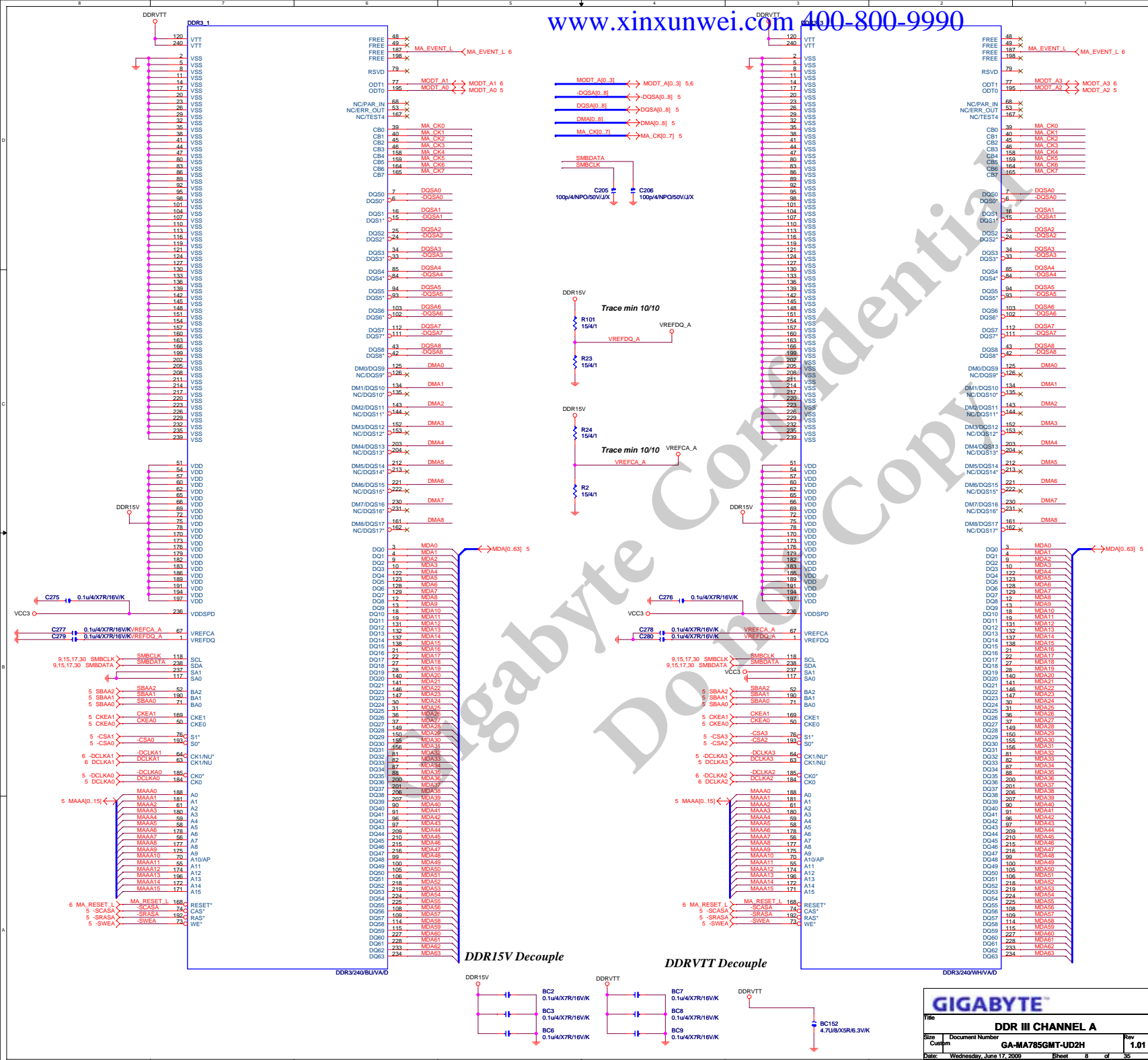
GIGABYTE™			
Title CPU HYPER TRANSPORT			
Size Custom	Document Number GA-MA785GMT-UD2H	Rev 1.01	
Date: Wednesday, June 17, 2009	Sheet 4	of 35	

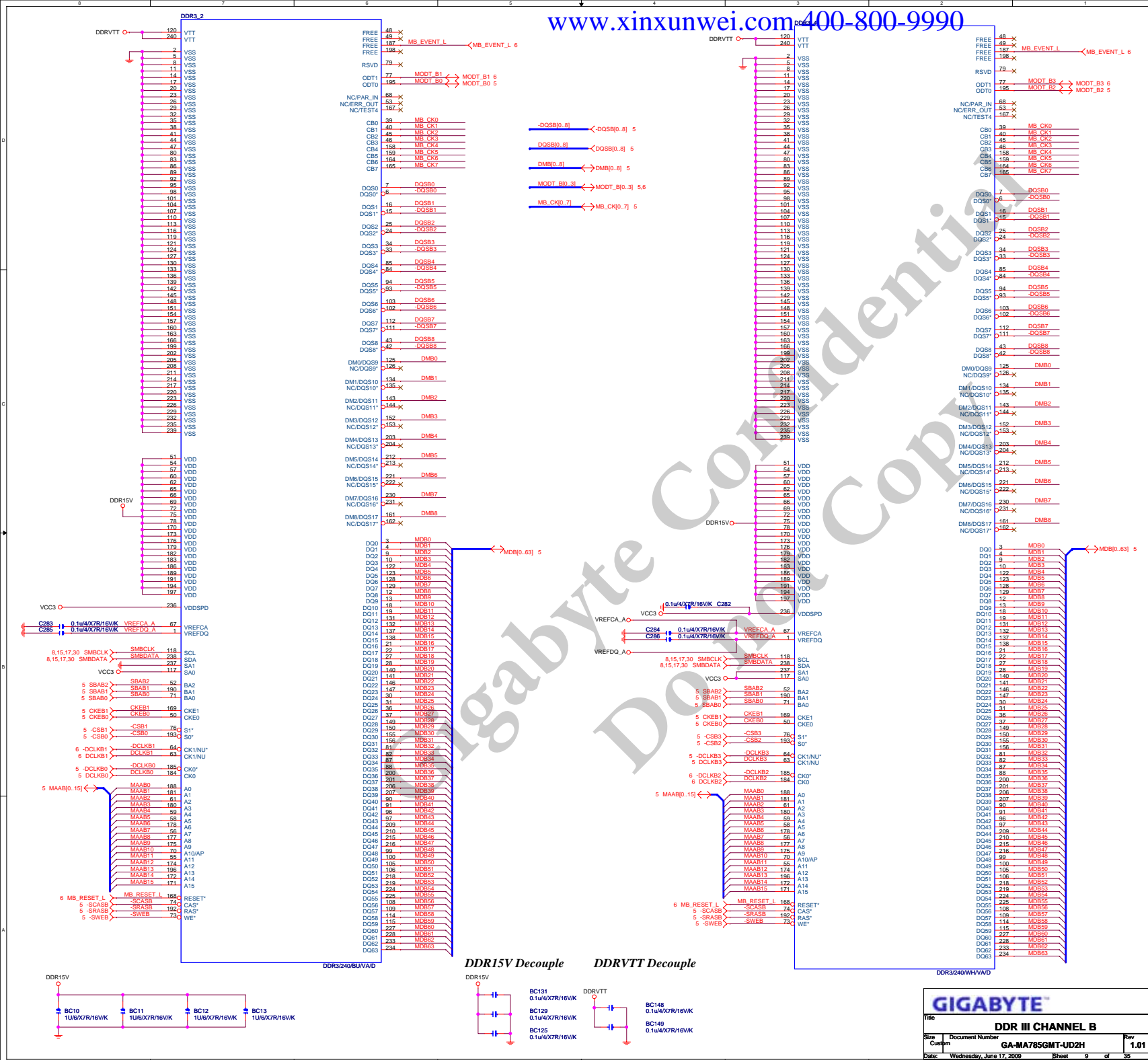


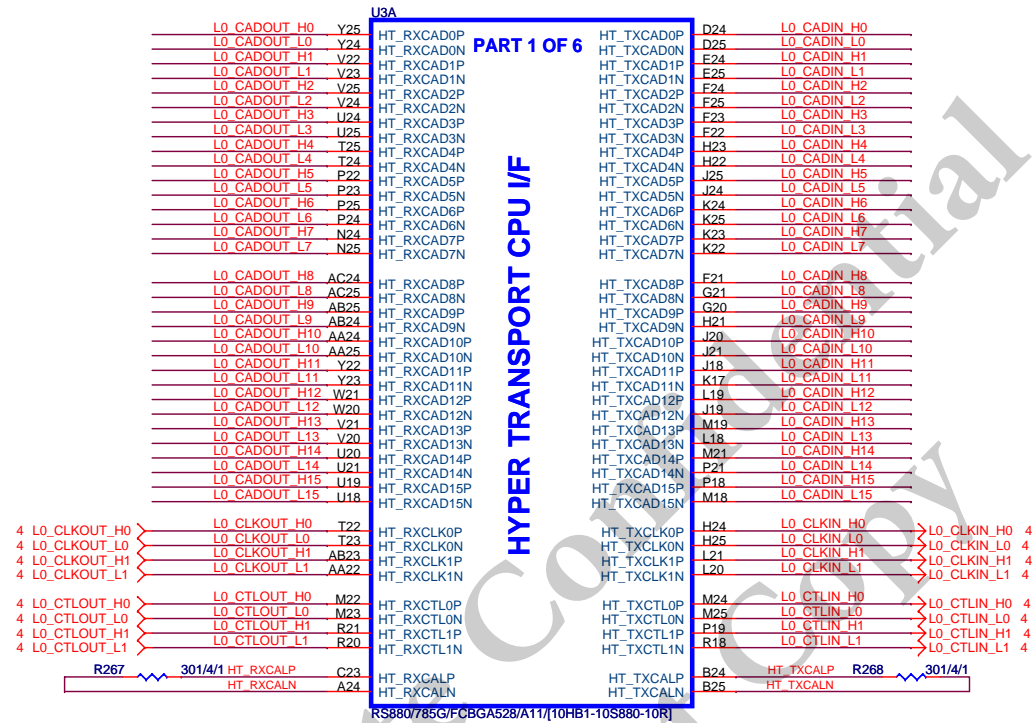


VLDT_RUN_B is connected to the VLDT_RUN power supply through the package or on the die. It is only connected on the board to decoupling near the CPU package.







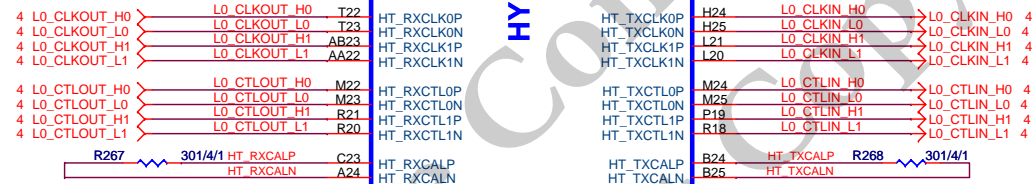


L0 CADIN L[0..15] < L0_CADIN_L[0..15] 4

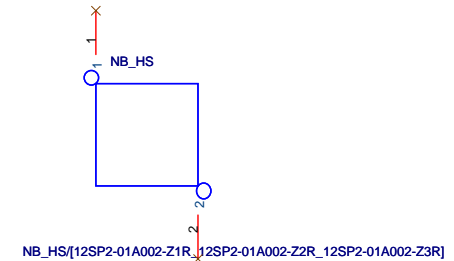
L0 CADIN H[0..15] < L0_CADIN_H[0..15] 4

L0 CADOUT L[0..15] < L0_CADOUT_L[0..15] 4

L0 CADOUT H[0..15] < L0_CADOUT_H[0..15] 4

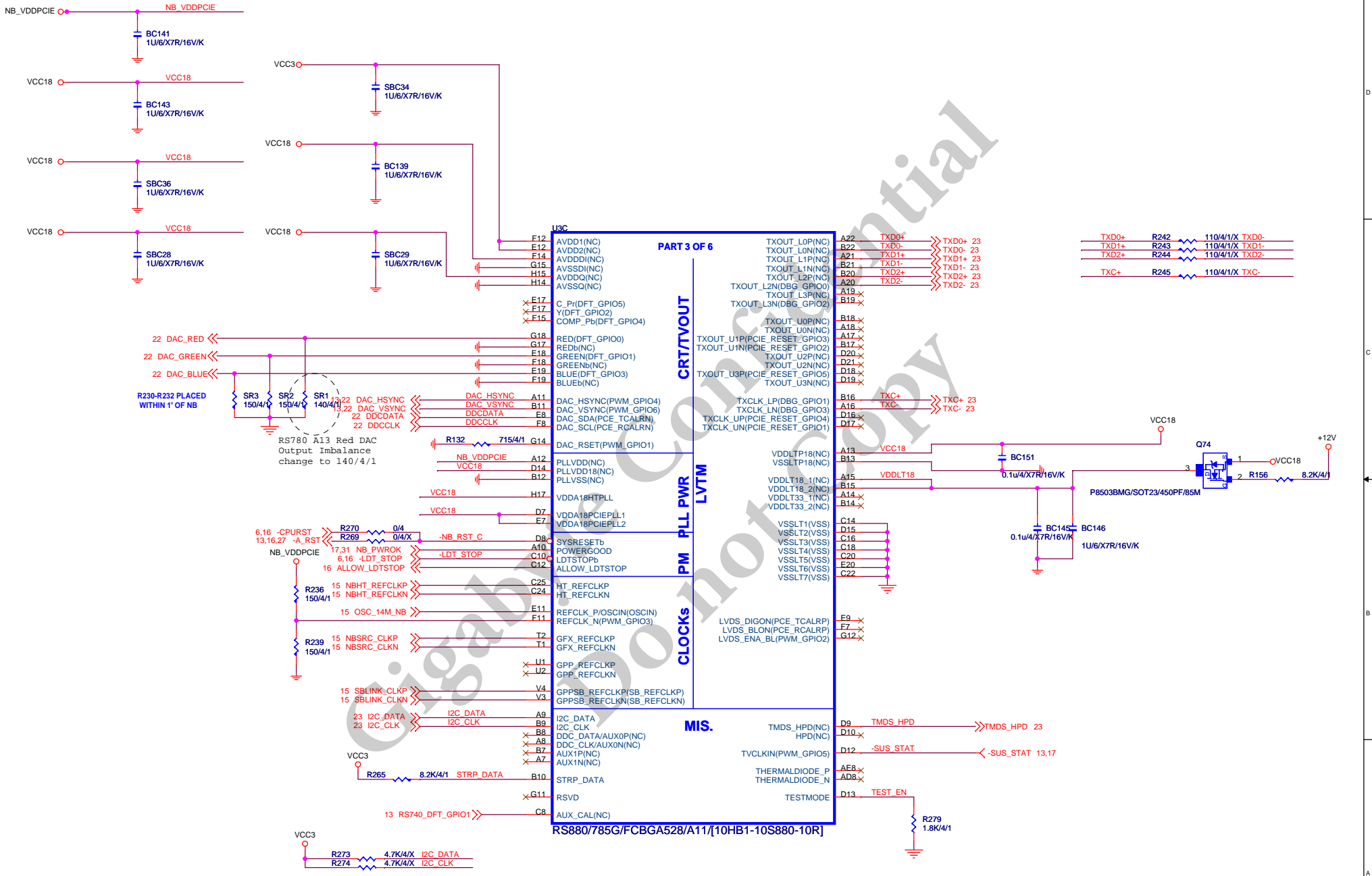


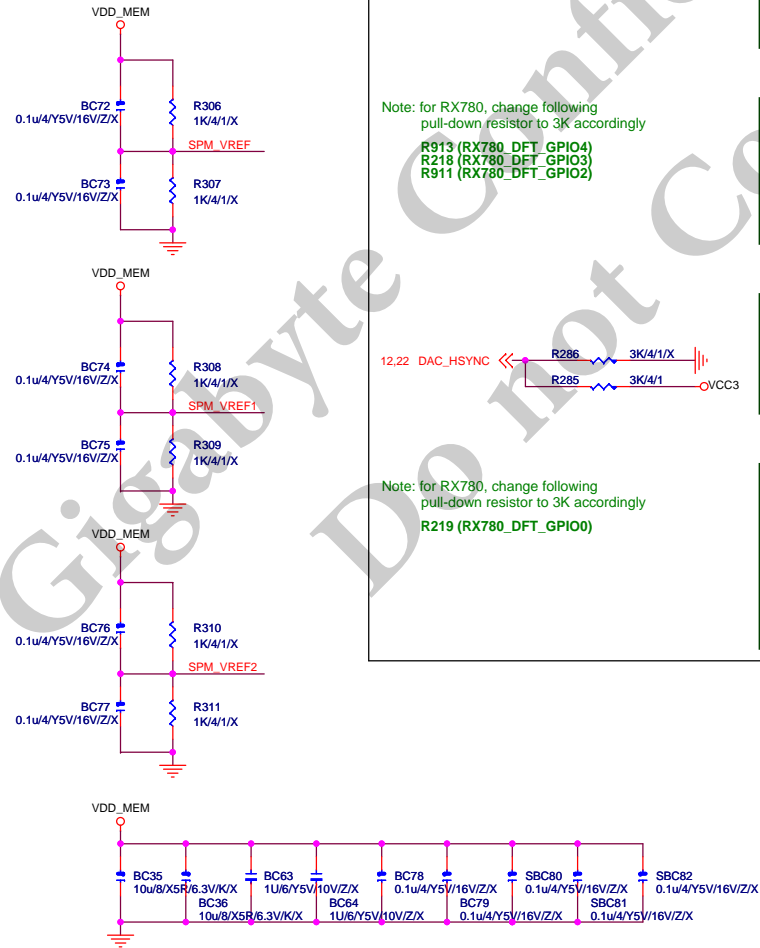
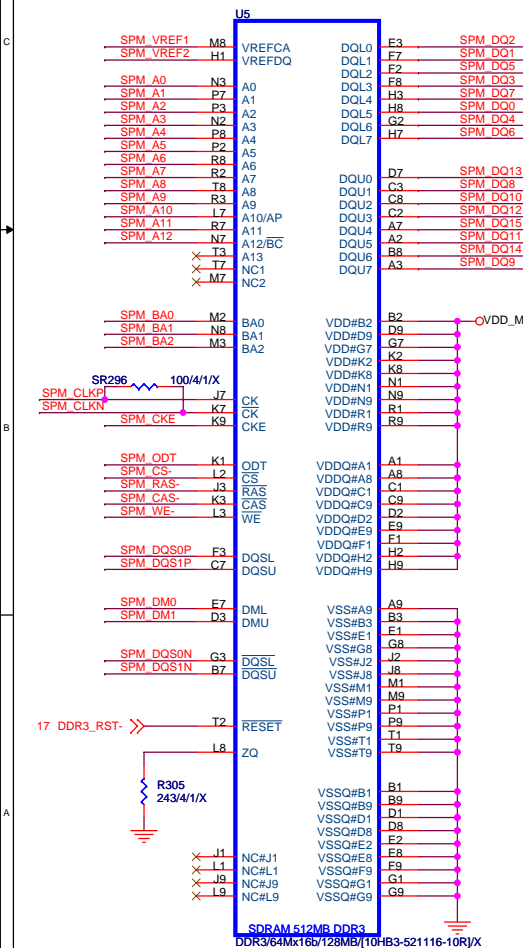
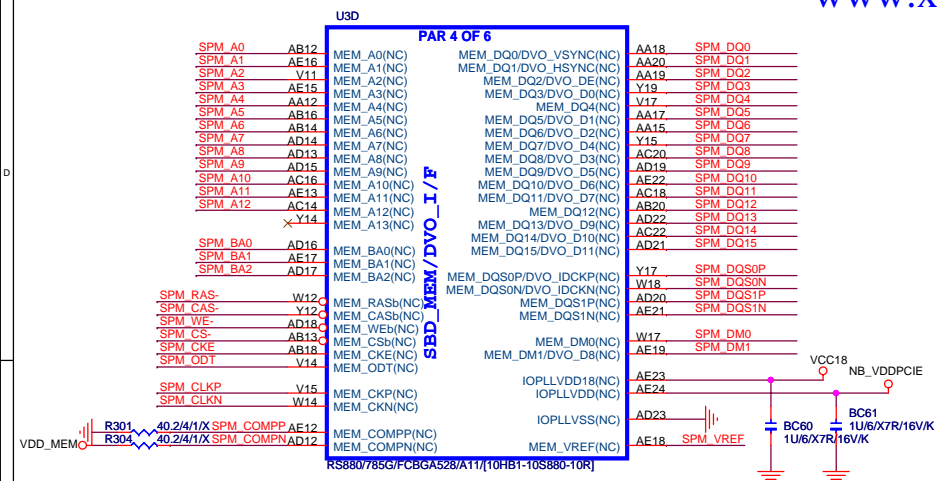
HT Link Stitching Caps

**GIGABYTE™**

Title		
RS880 HT-LINK I/F		
Size	Document Number	Rev
B	GA-MA785GMT-UD2H	1.01
Date:	Wednesday, June 17, 2009	Sheet 10 of 35





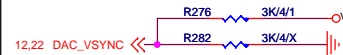


RS740/RX780/RS780 STRAPS

Note: for RS780, change R232 to 150R as AUX_CAL,
place close to pin C8



Note: for RX780, R217 (RX780_DFT_GPIO1) to 3K according



Note: for RX780, change following pull-down resistor to 3K accordingly
R912 (RX780_DFT_GPIO5)

```
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
  default values if not connected
RS740: pin DFT_GPIO1
RX780: pin DFT_GPIO1
RS780: pin SUS_STAT#
```

RS740/RX780/RS780: STRAP_DEBUG_BUS_GPIO_ENABLE

```

Enables the Test Debug Bus using GPIO and/or memory IO
1 : Disable (RS740/RS780); Enable (RX780)
0 : Enable (RS740/RS780); Disable(RX780)
RS740: pin DFT_GPIO5
RX780: pin DFT_GPIO5
RS780: pin VSYNC

```

RS740: STRAP_PCIE_SB/GPP_CFG[2:0] (Pins: RS740_DFT_GPIO[4:2])

```

These pin straps are used to configure PCI-E GPP mode.
111: register defined (register default to Config E) default
110: 4-0-0-0-0 Config A
101: 4-4-0-0-0 Config B
100: 4-2-2-0-0 Config C
011: 4-2-1-1-0 Config D
010: 4-1-1-1-1 Config E
others: register defined (default to Config E)

```

RX780: STRAP_PCIE_GPP_CFG[2:0] (Pins: RX780_DFT_GPIO[4:2])

```
111: 1-1-1-1-1-1 Mode L default
110: 1-1-1-1-1-1 Mode L
101: 2-0-2-0-2-0 Mode C2
100: 2-0-2-0-1-1 Mode K
011: 2-0-1-1-1-1 Mode E
010: 1-1-1-1-1-1 Mode L
001: 4-0-0-0-1-1 Mode C
000: 4-0-0-0-2-0 Mode B
```

RS780: STRAP_PCIE_GPP_CFG[2:0]
(configure thru register setting)

1-1-1-1-1-1	Mode L	default
1-1-1-1-1-1	Mode L	
2-0-2-0-2-0	Mode C2	
2-0-2-0-1-1	Mode K	
2-0-1-1-1-1	Mode E	
1-1-1-1-1-1	Mode L	
4-0-0-0-1-1	Mode C	
4-0-0-0-2-0	Mode B	

RS740/RX780/RS780: SIDE-PORT MEMORY ENABLE

```
Enables Side port memory
1. Disable (RS740/RS780)
0 : Enable (RS740/RS780)
RS740: pin DFT_GPIO0
RS780: pin HSYNC
RX780: Not Applicable
```

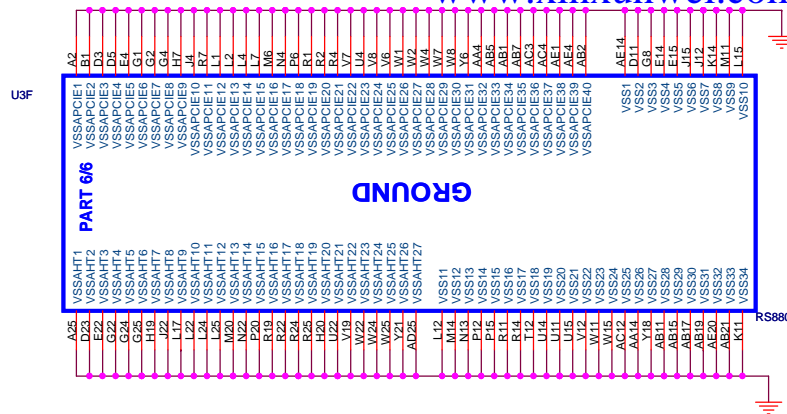
RX780/RS780: STRAP_DEBUG_BUS_PCIE_ENABLE

```
Enables Test debug bus
using PCIE bus
1. Disable (can be enabled
   thru nbcbfg register)
0 : Enable
RX780: pin DFT_GPI00
RS780: configurable thru register
      setting only
RS740: Not supported
```

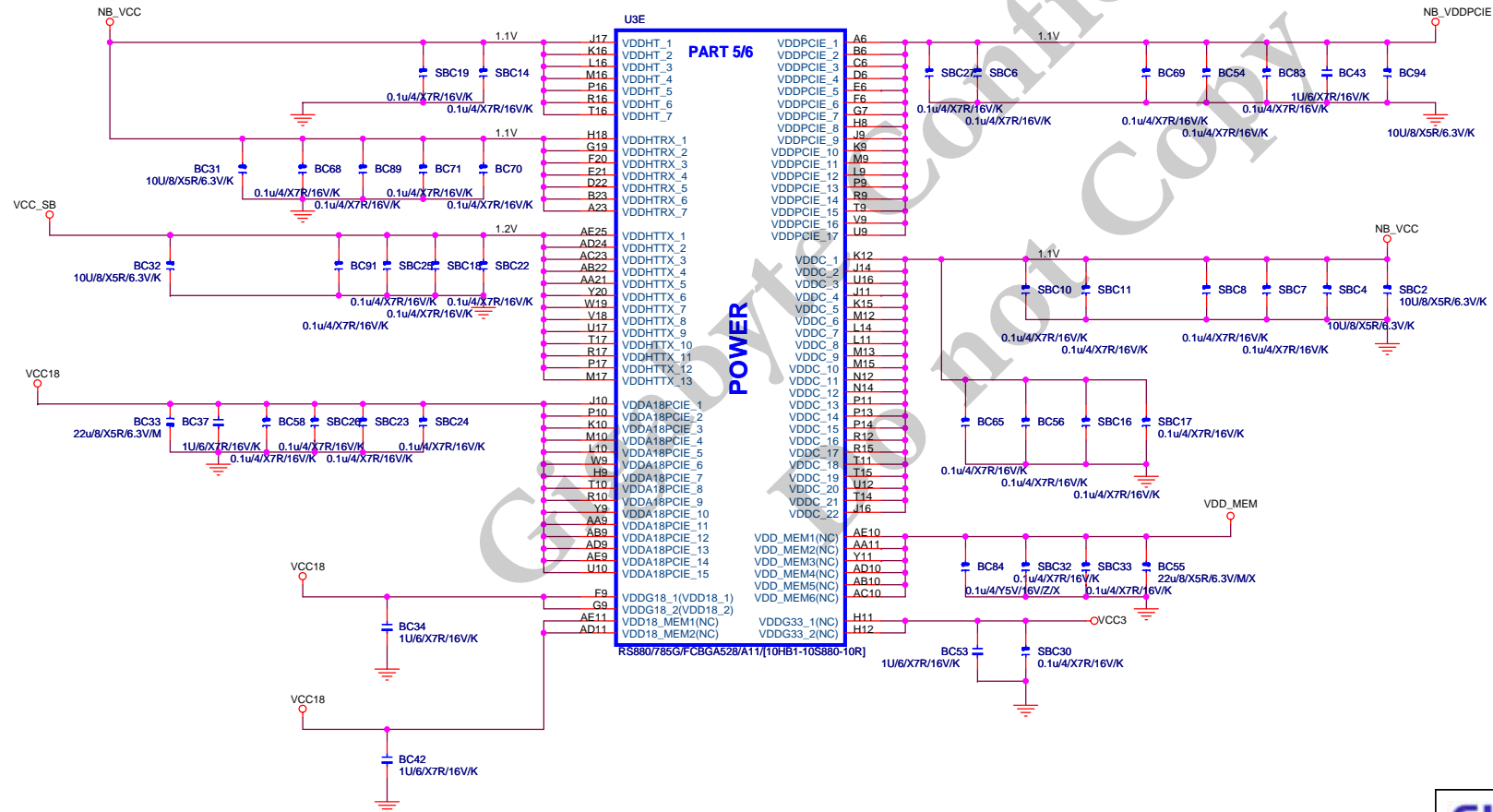
Note: for RX780, change following pull-down resistor to 3K accordingly
R219 (RX780_DFT_GPIO0)



PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V	NC	+1.8V(DDR2) +1.5V(DDR3)	VDDLTP18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDL18	+1.8V	NC	+1.8V
IOPLLVD18	+1.8V	NC	+1.8V	VDDL33	+3.3V	NC	NC



Please use 1mm pad size,
place all ELT test pads
on bottom side only



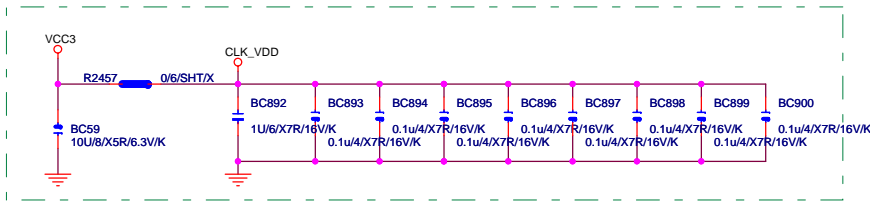
GIGABYTE™

Title			RS880 POWER & GND
Size	Document Number	Rev	1.01
Custom	GA-MA785GMT-UD2H		
Date:	Wednesday, June 17, 2009	Sheet	14 of 35

NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF	100M DIFF
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPPSB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

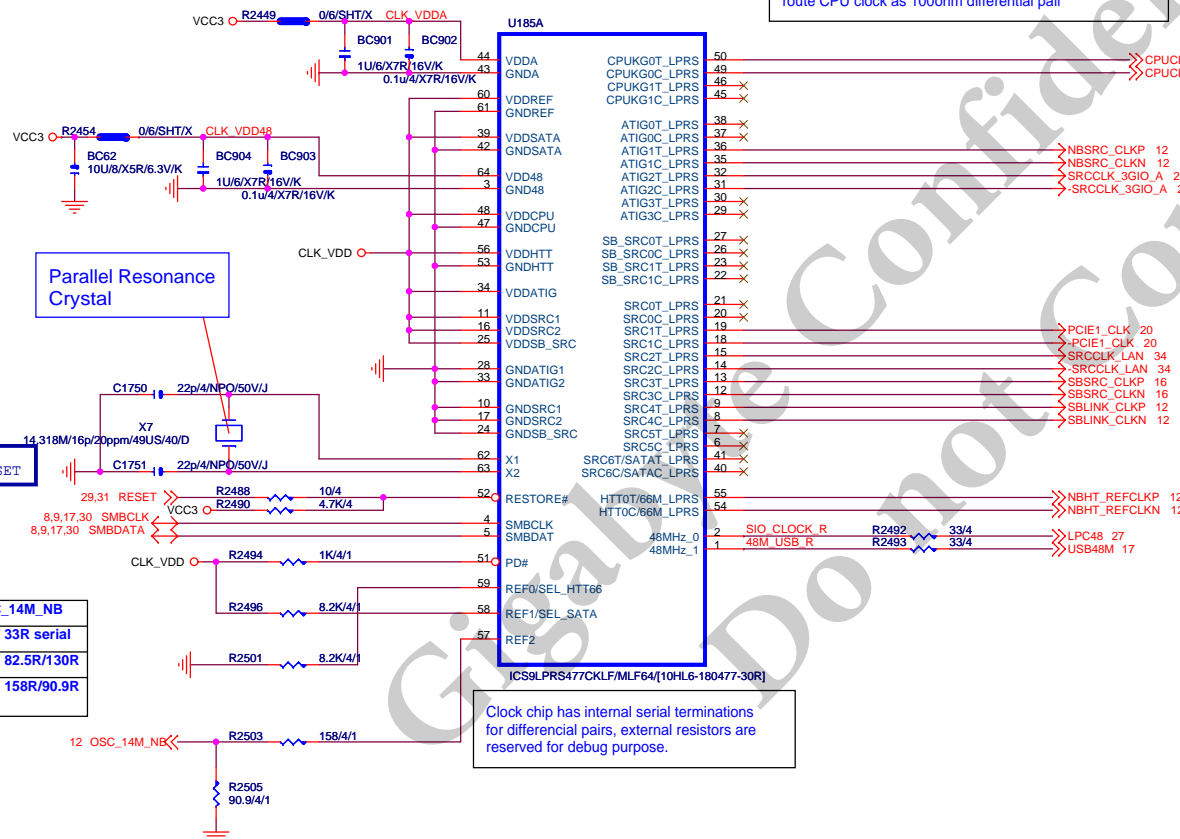
* the GFX_REFCLK input is required for all cases



- 1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE TO U800 AS POSSIBLE
- 2- ROUTE ALL SRCCLKTx AND SRCCLKCx AS DIFFERENT PAIR RULE
- 3- PUT DECOUPLING CAPS CLOSE TO U800 POWER PIN



Place R800/801 less than 500 mils away from U800
R851 less than 100 mils away from R800/801
route CPU clock as 100ohm differential pair



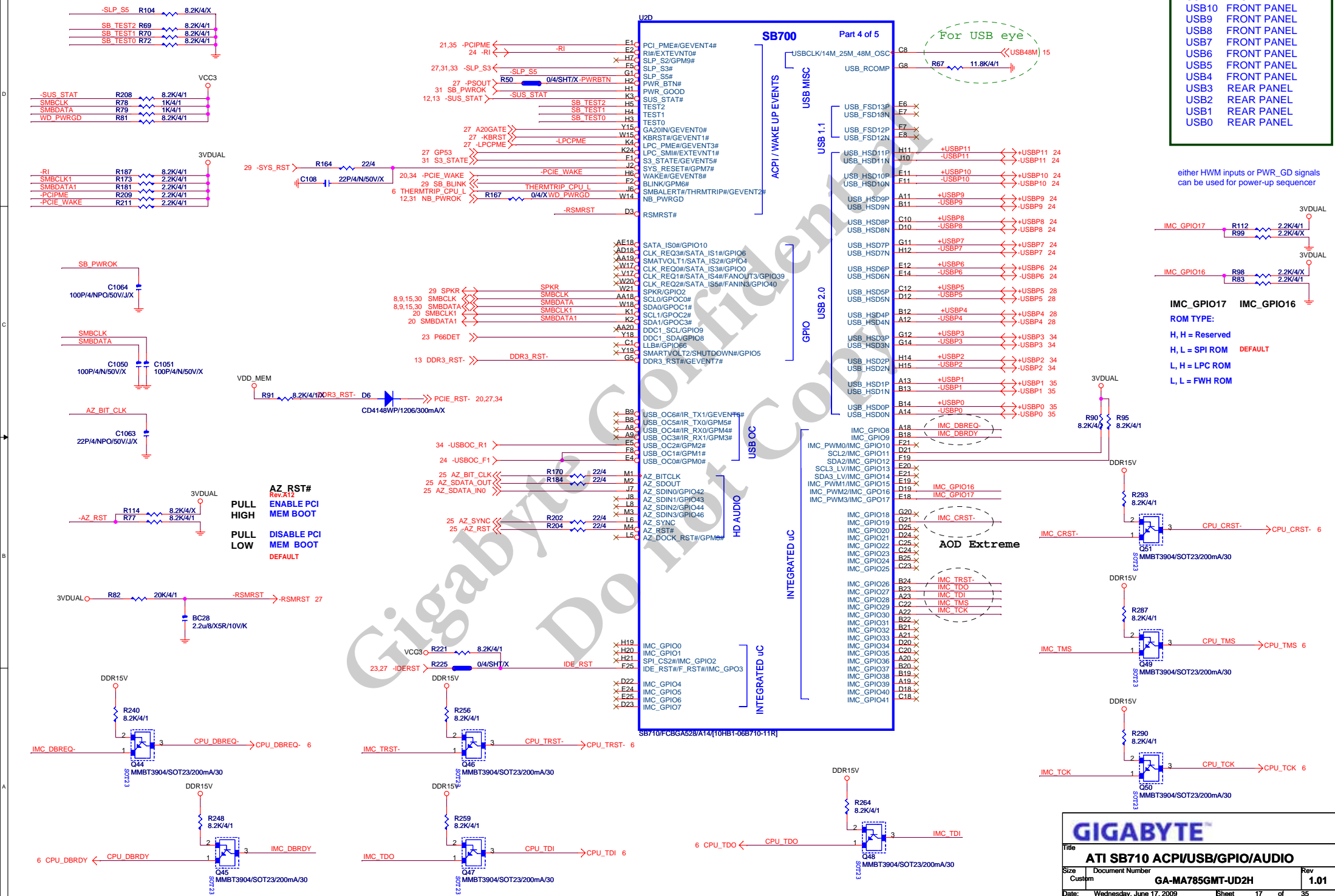
	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

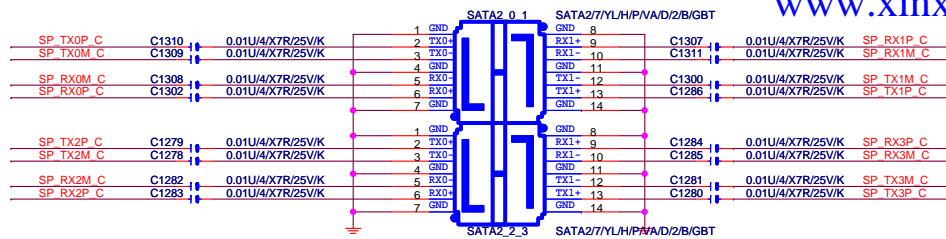
REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK

USB11	FRONT PANEL
USB10	FRONT PANEL
USB9	FRONT PANEL
USB8	FRONT PANEL
USB7	FRONT PANEL
USB6	FRONT PANEL
USB5	FRONT PANEL
USB4	FRONT PANEL
USB3	REAR PANEL
USB2	REAR PANEL
USB1	REAR PANEL
USB0	REAR PANEL

either HWM inputs or PWR_GD signals
can be used for power-up sequencer





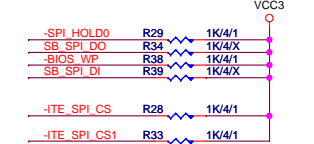
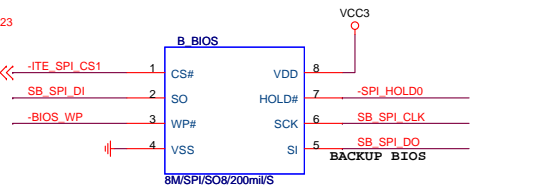
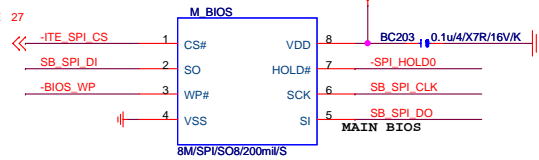
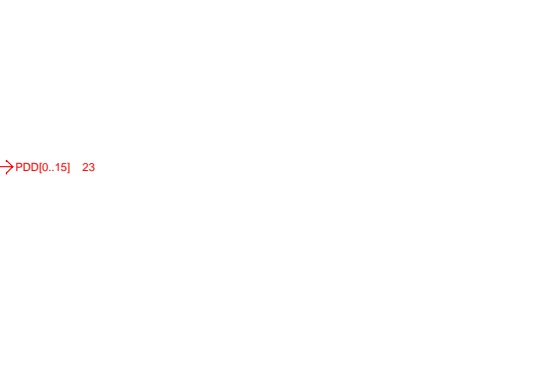
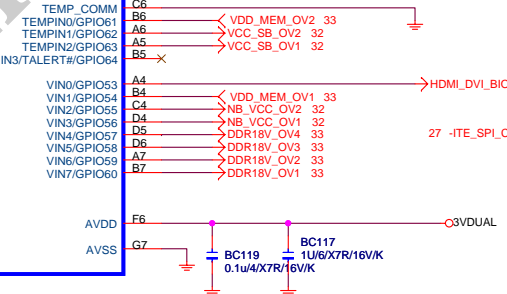
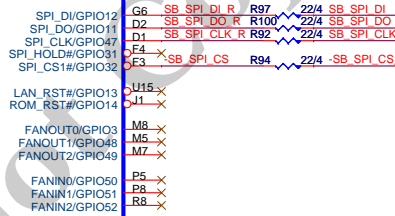
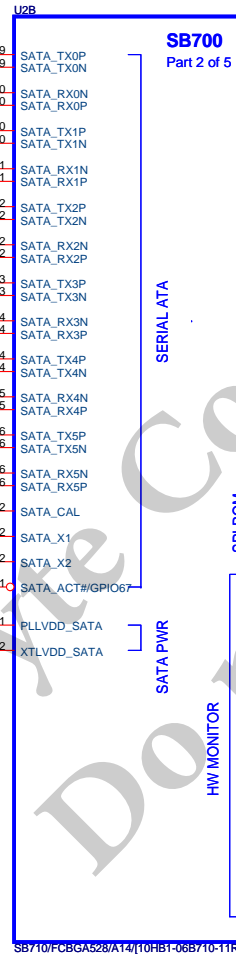
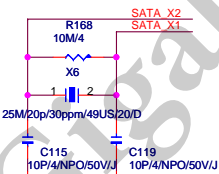
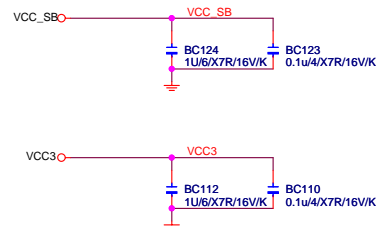
PLACE SATA AC COUPLING
CAPS CLOSE TO SB600



PLACE SATA CAL
RES VERY CLOSE
TO BALL OF U600

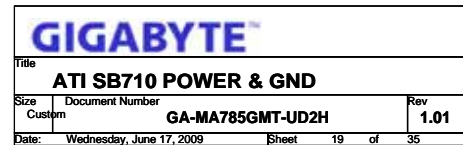
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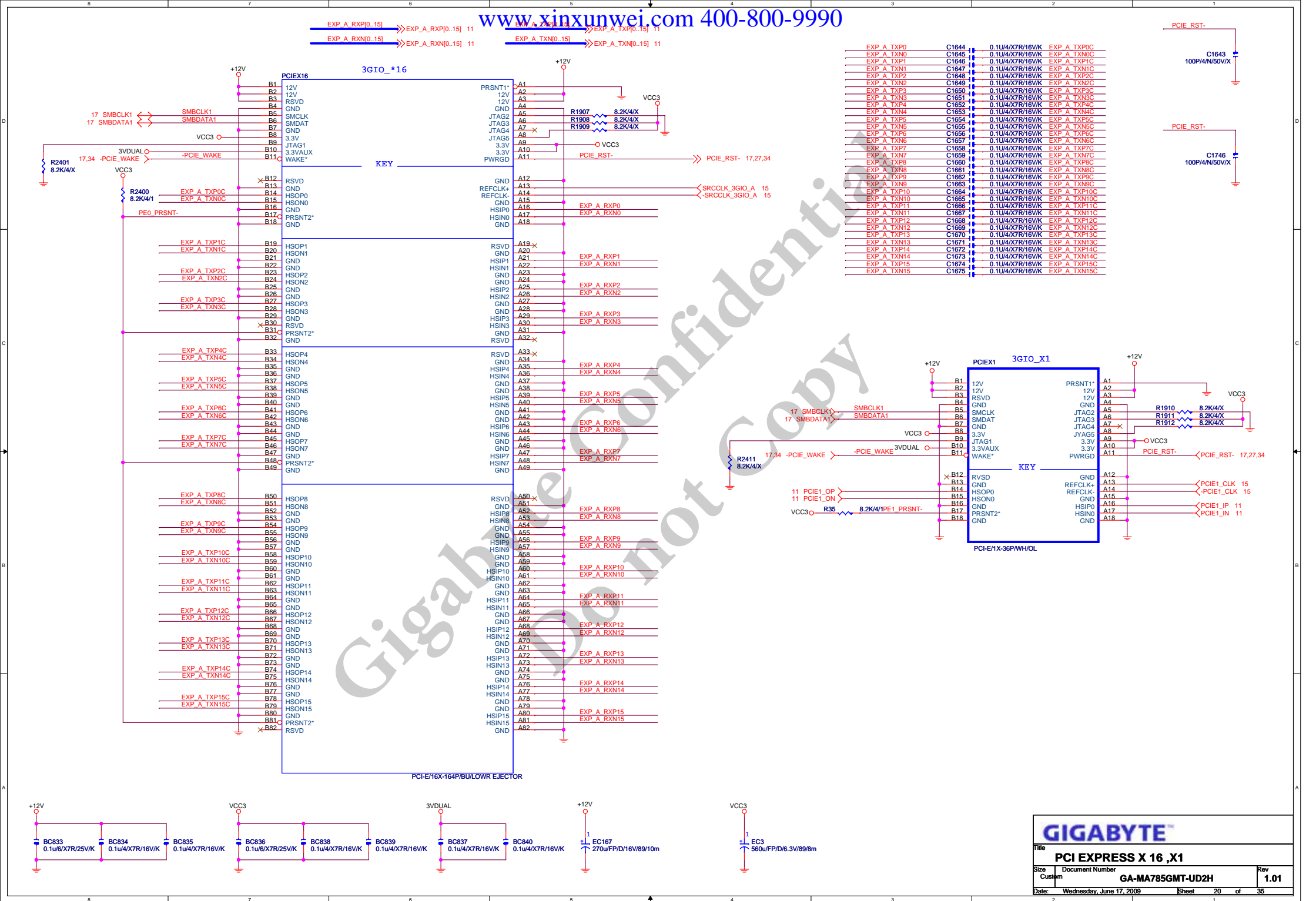
R650 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK



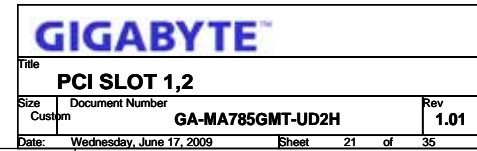
GIGABYTE

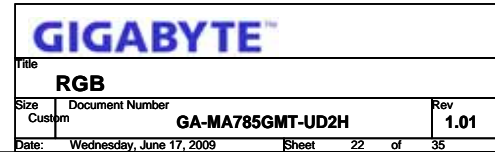
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Size	Document Number	Rev
Custom	GA-MA785GMT-UD2H	1.01
Date:	Wednesday, June 17, 2009	Sheet 18 of 35

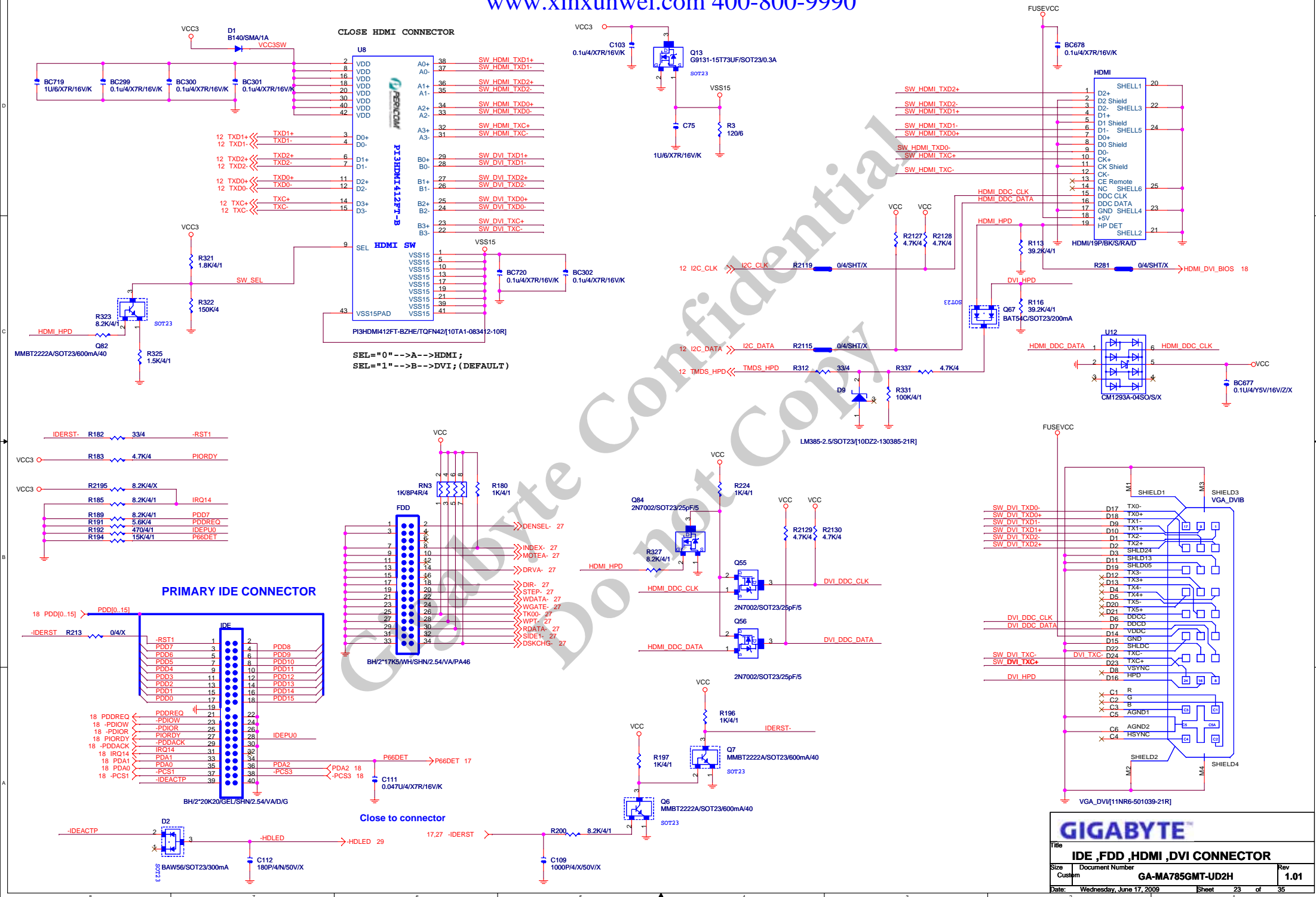


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PCI EXPRESS X 16 ,X1Document Number
GA-MA785GMT-UD2H
Rev
1.01

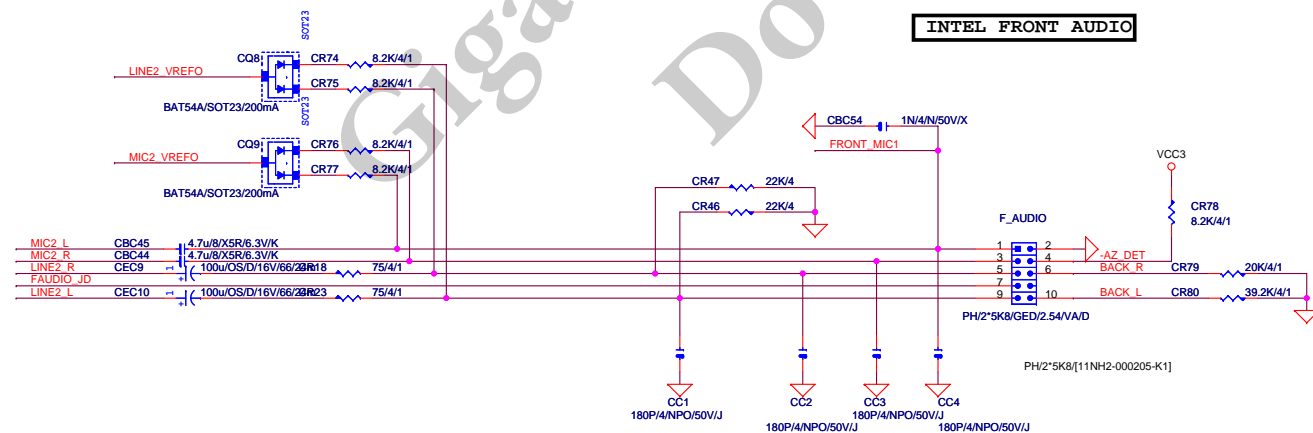
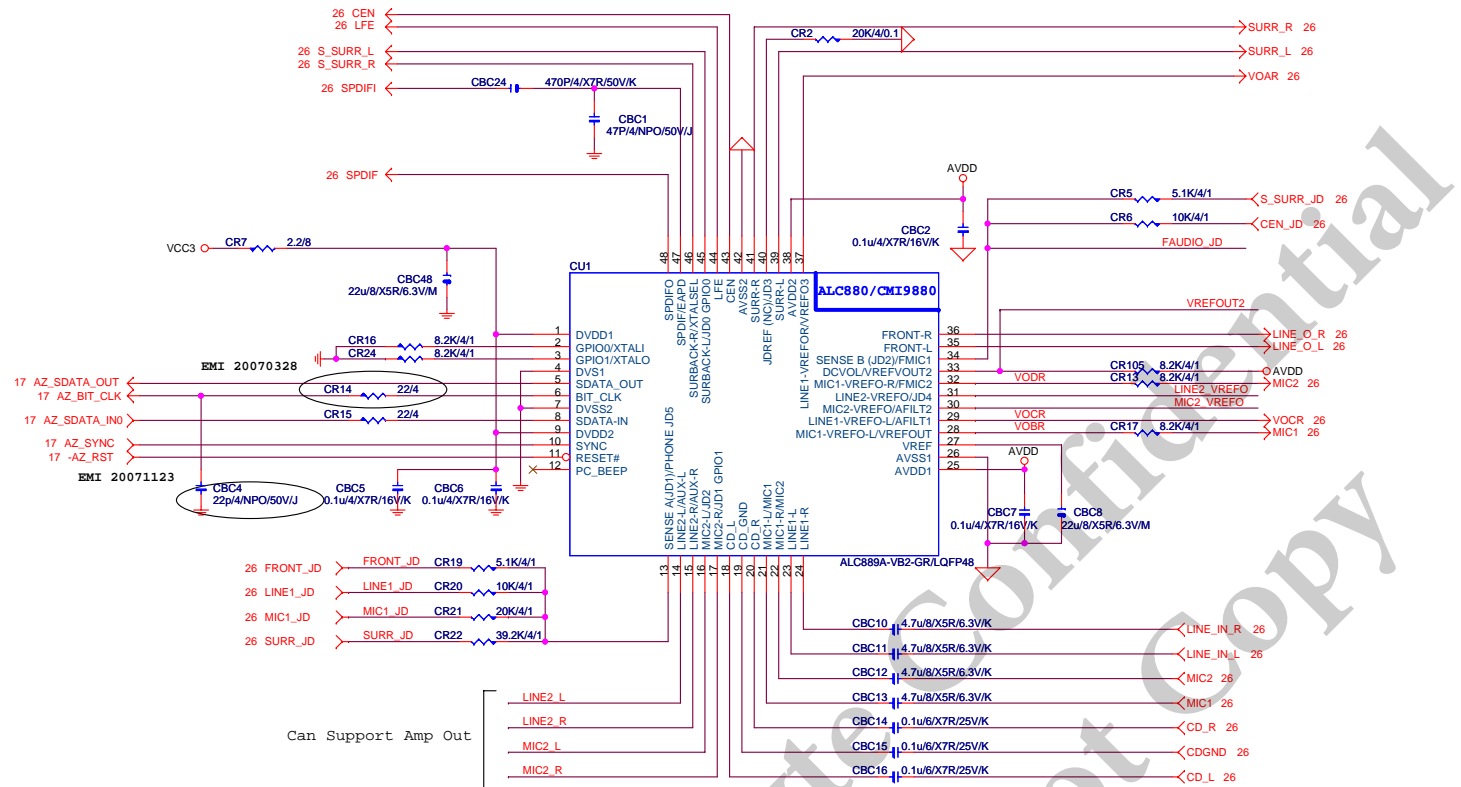
Date: Wednesday, June 17, 2009 Sheet 20 of 35





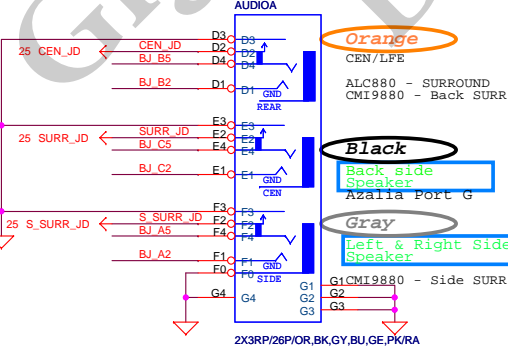
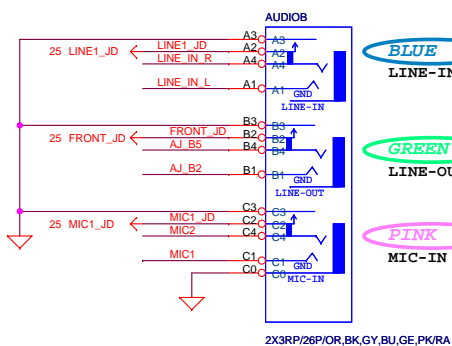
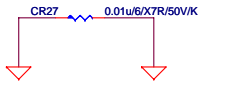
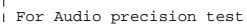
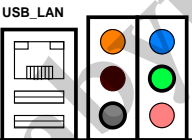
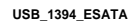
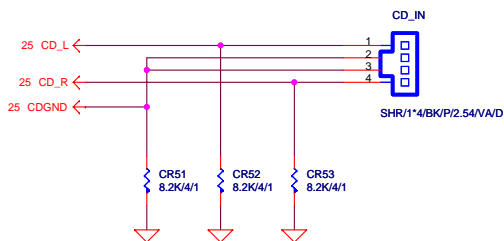
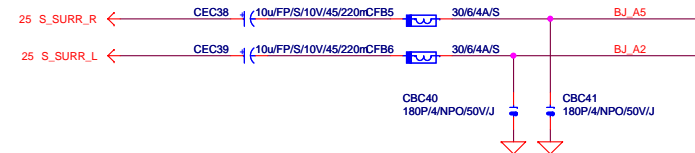
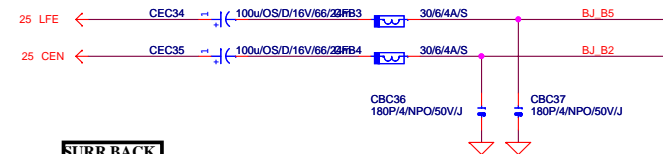
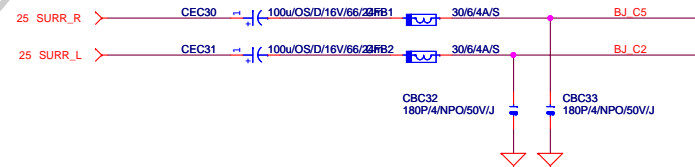
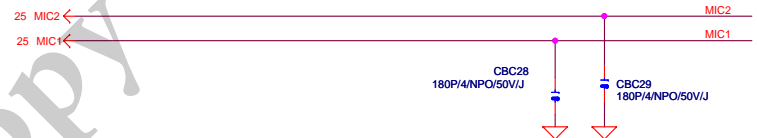
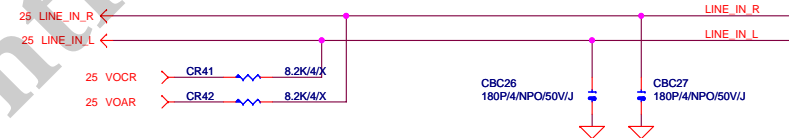
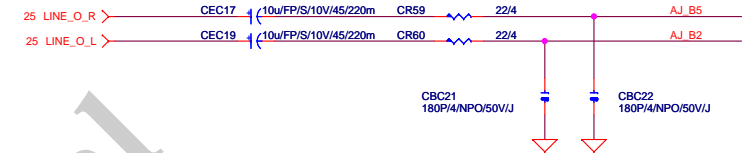
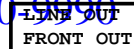
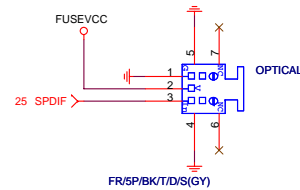
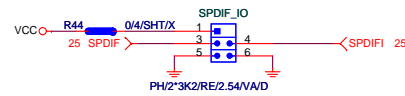
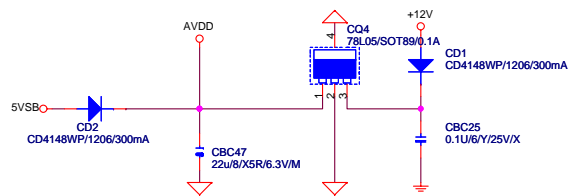
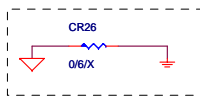


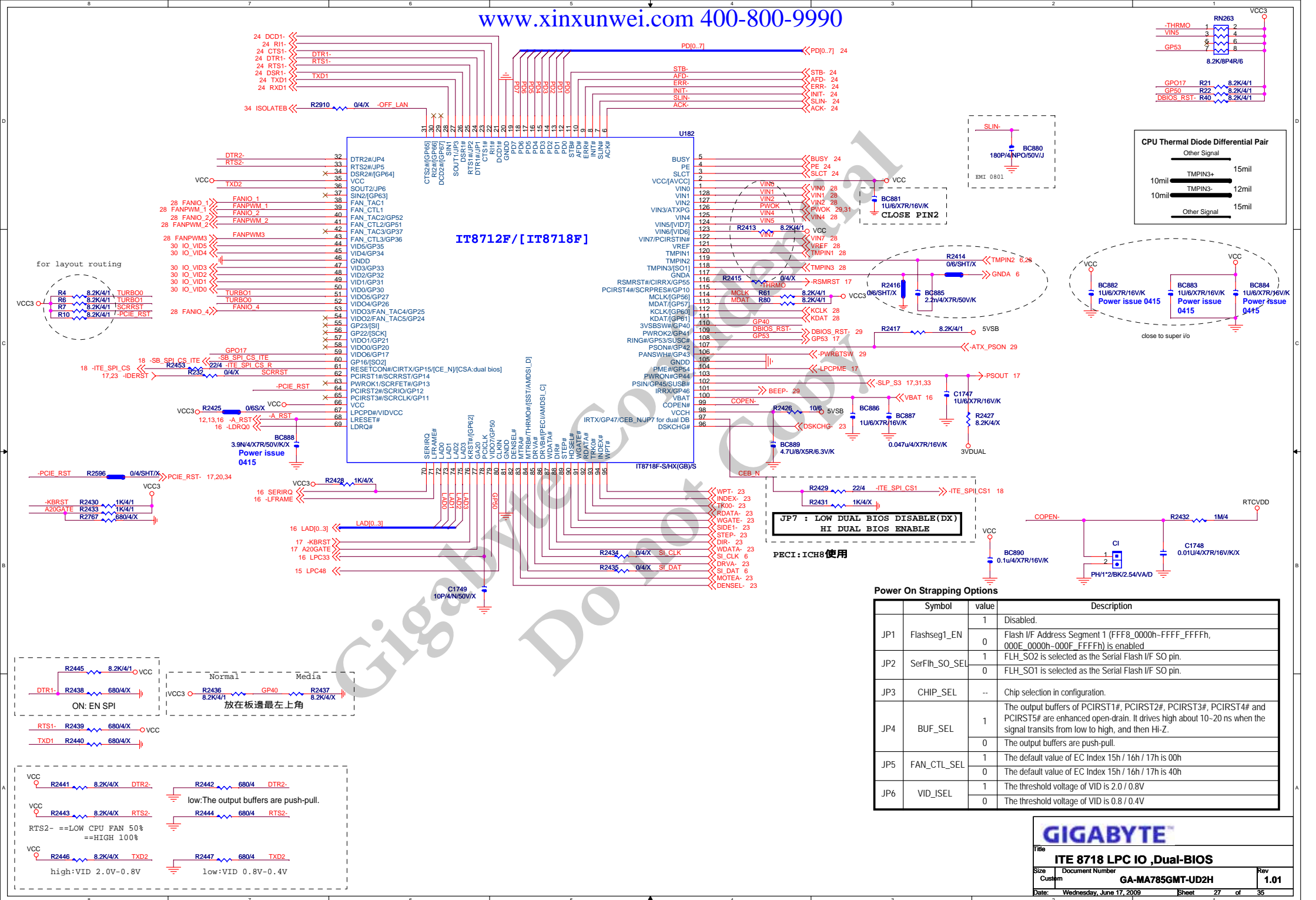




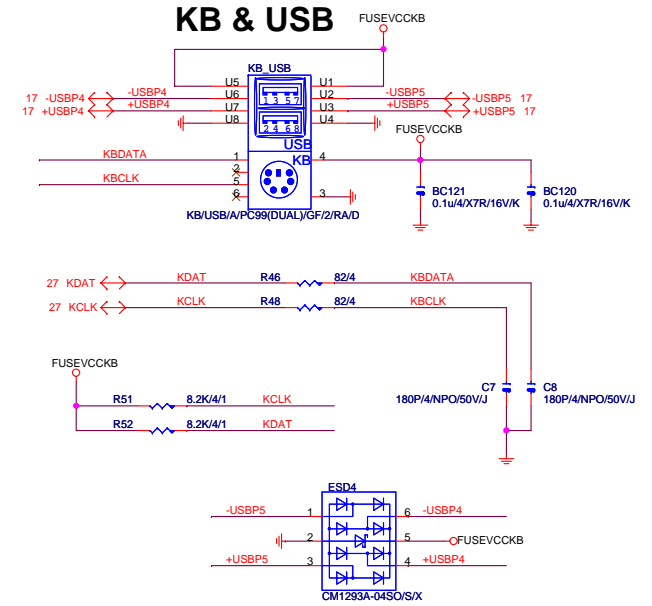
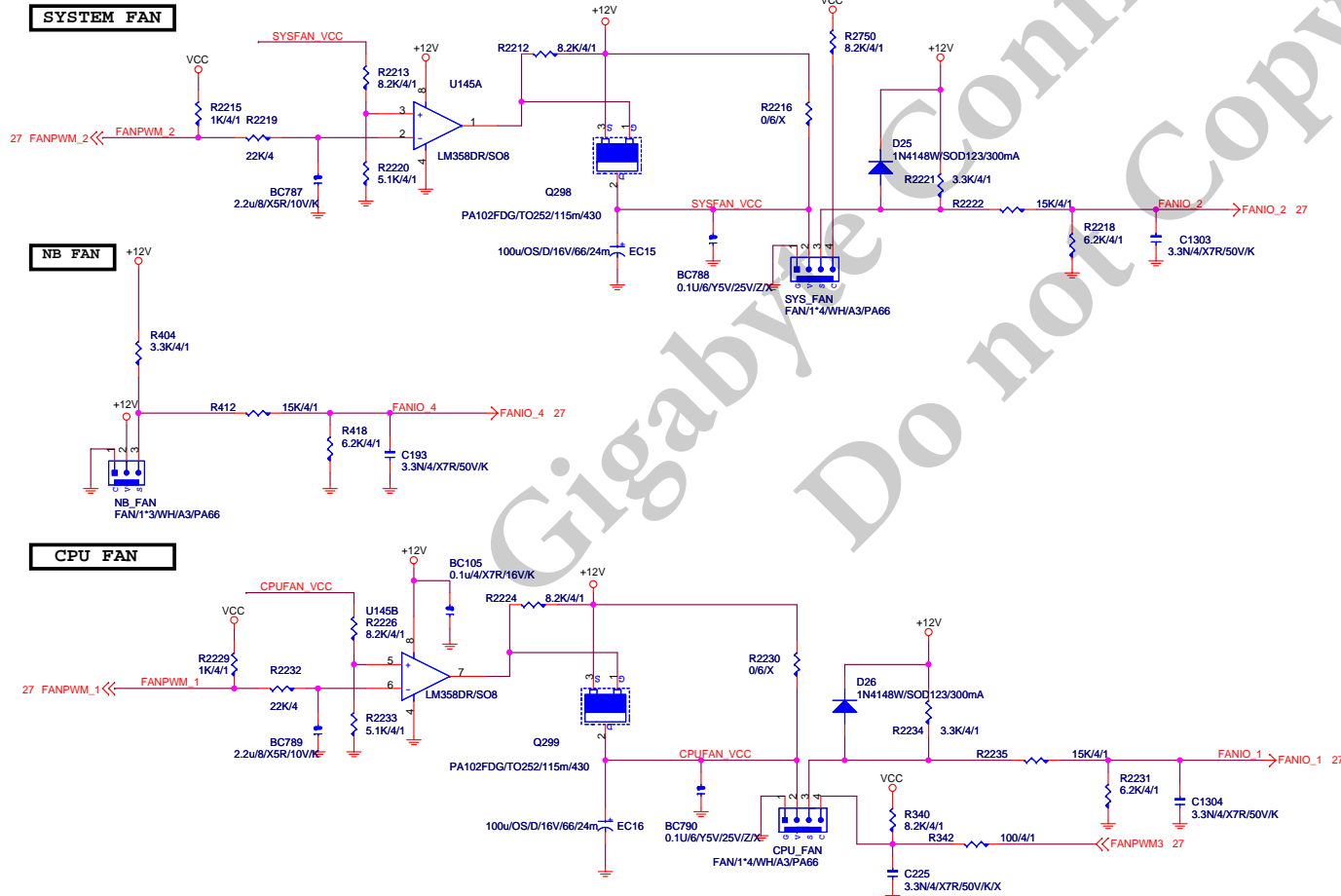
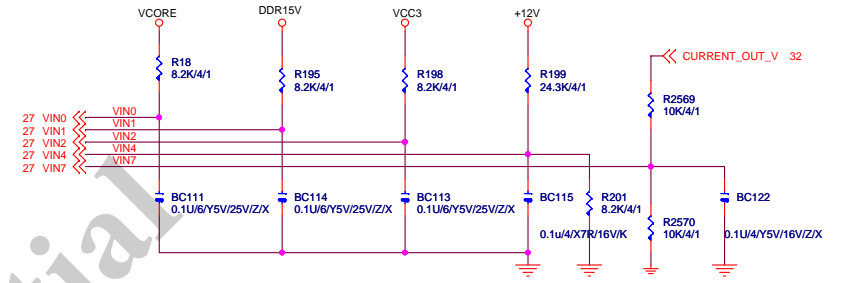
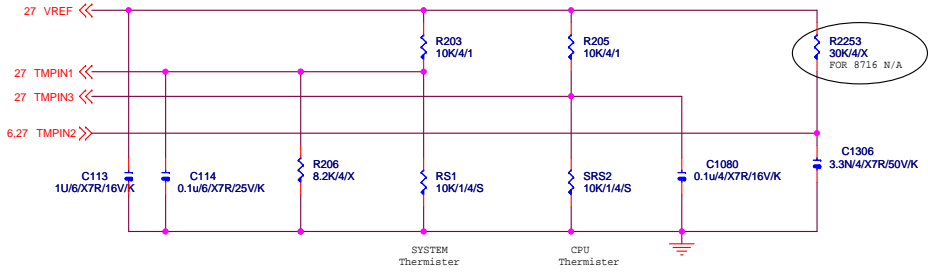
INTEL FRONT AUDIO

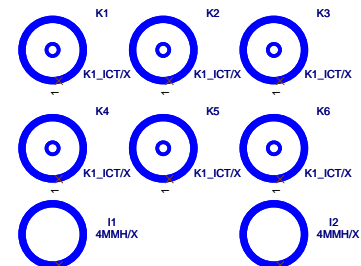
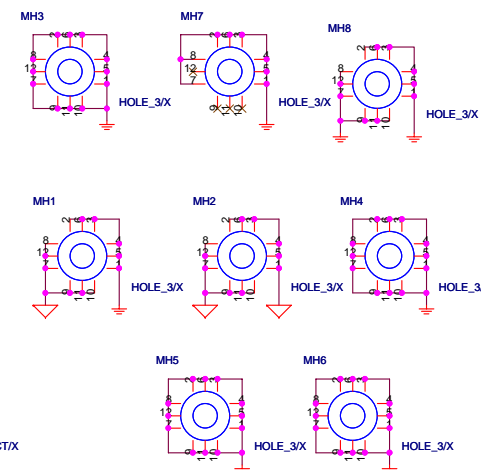
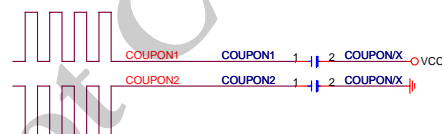
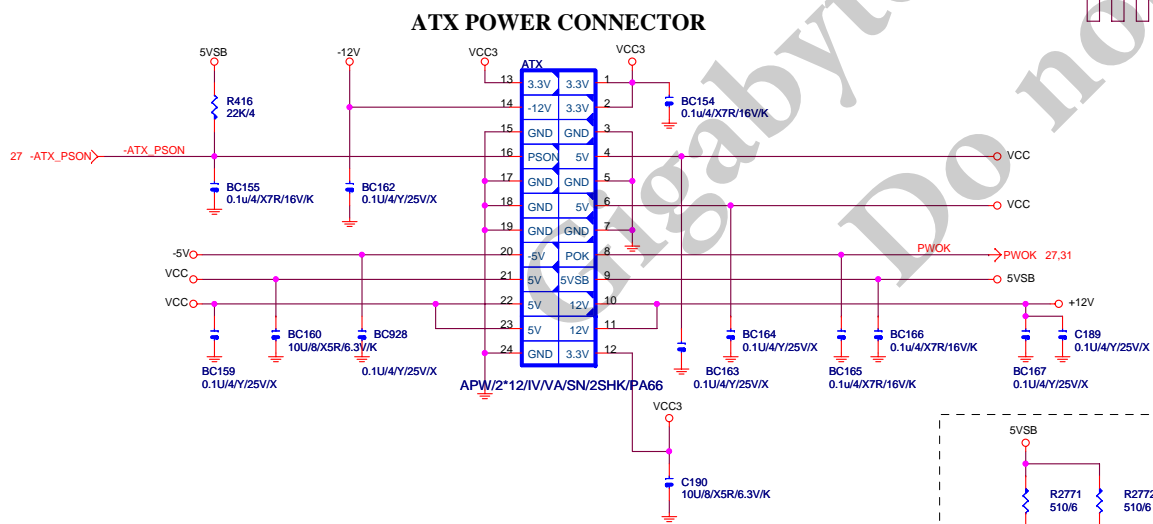
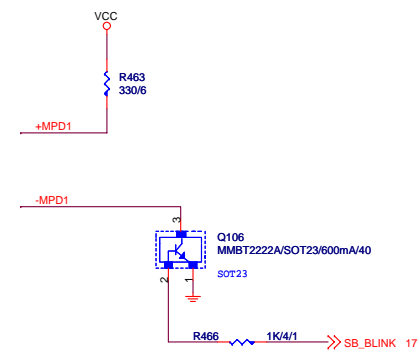
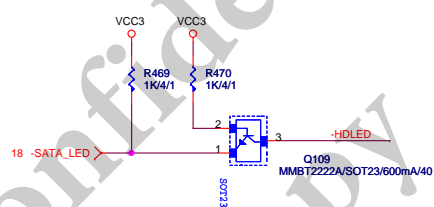
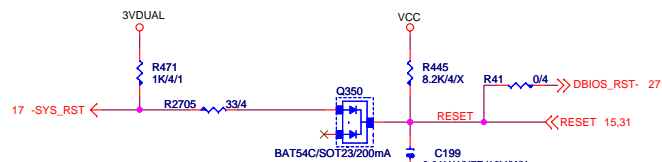
GIGABYTE™			
Title ALC889A CODEC			
Size	Document Number	Rev	
Custom	GA-MA785GMT-UD2H	1.01	
Date:	Wednesday, June 17, 2009	Sheet	25 of 35



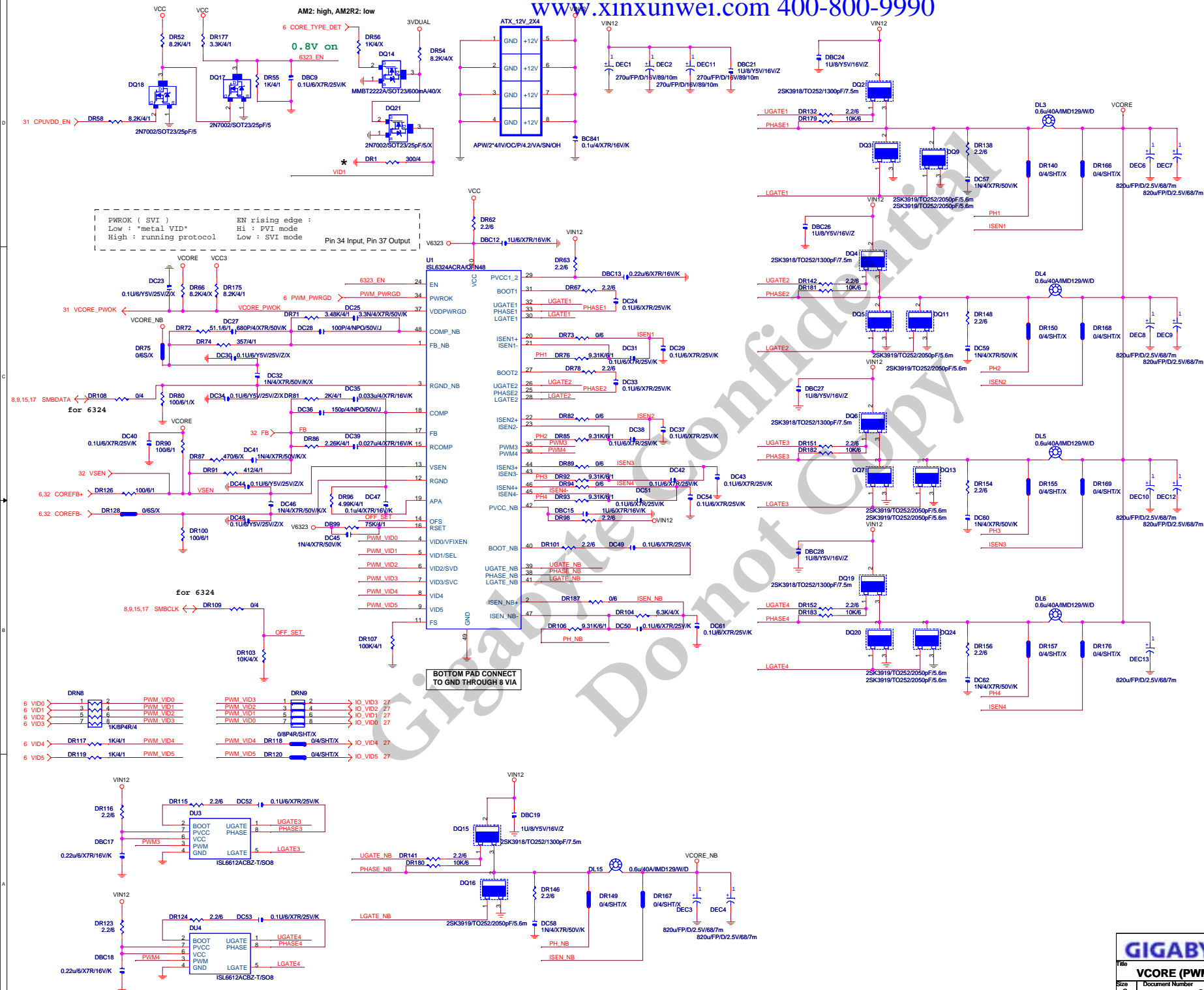


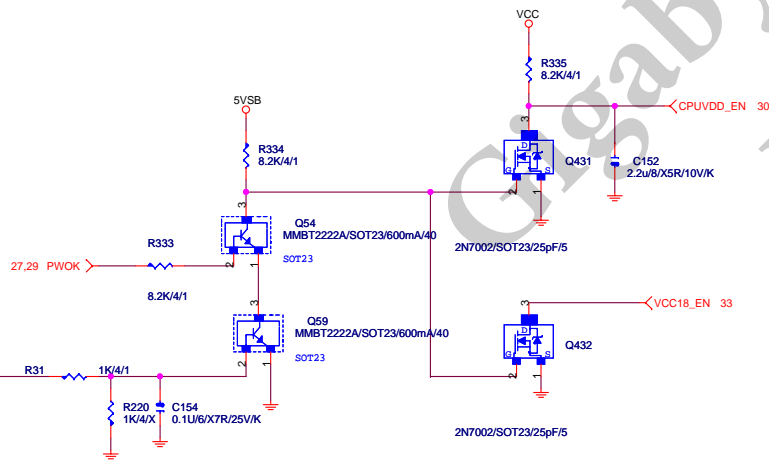
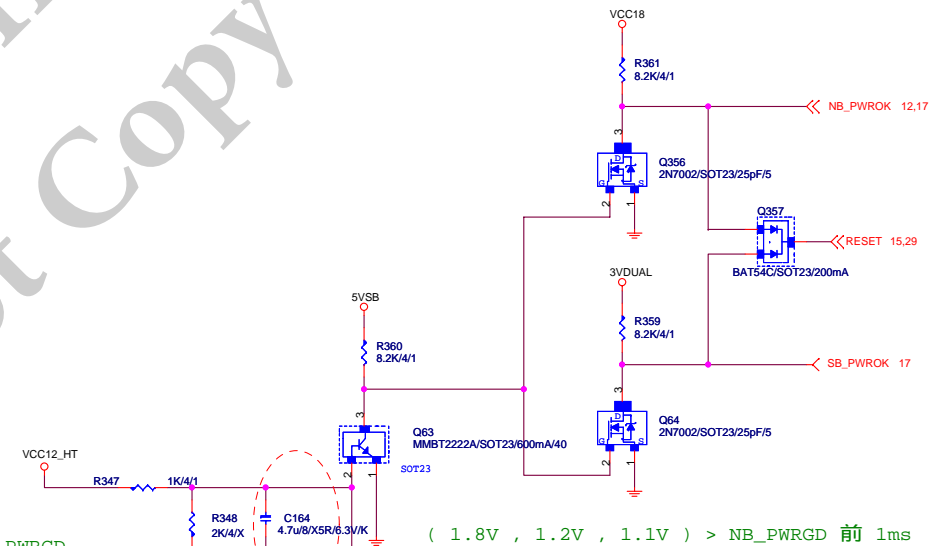
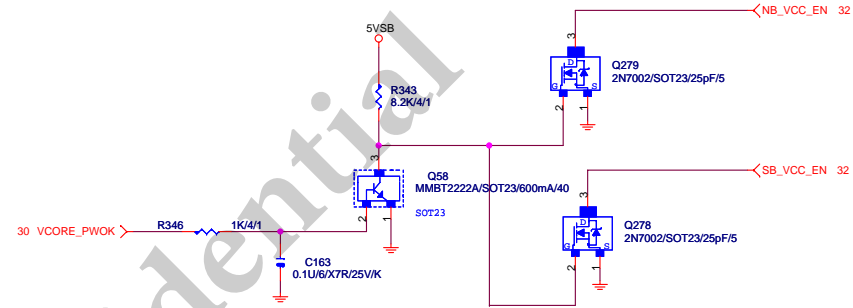
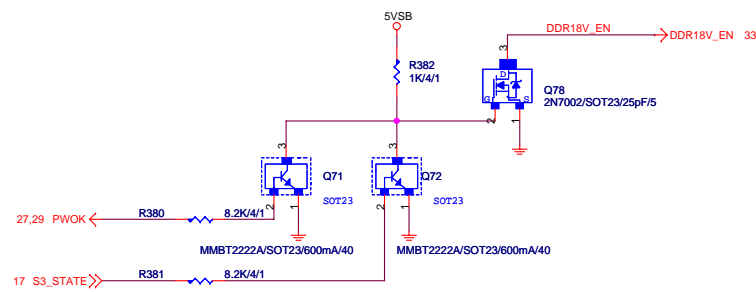
Hardware Monitor circuits





For Seasonic 900W
Power supply
cant Boot issue





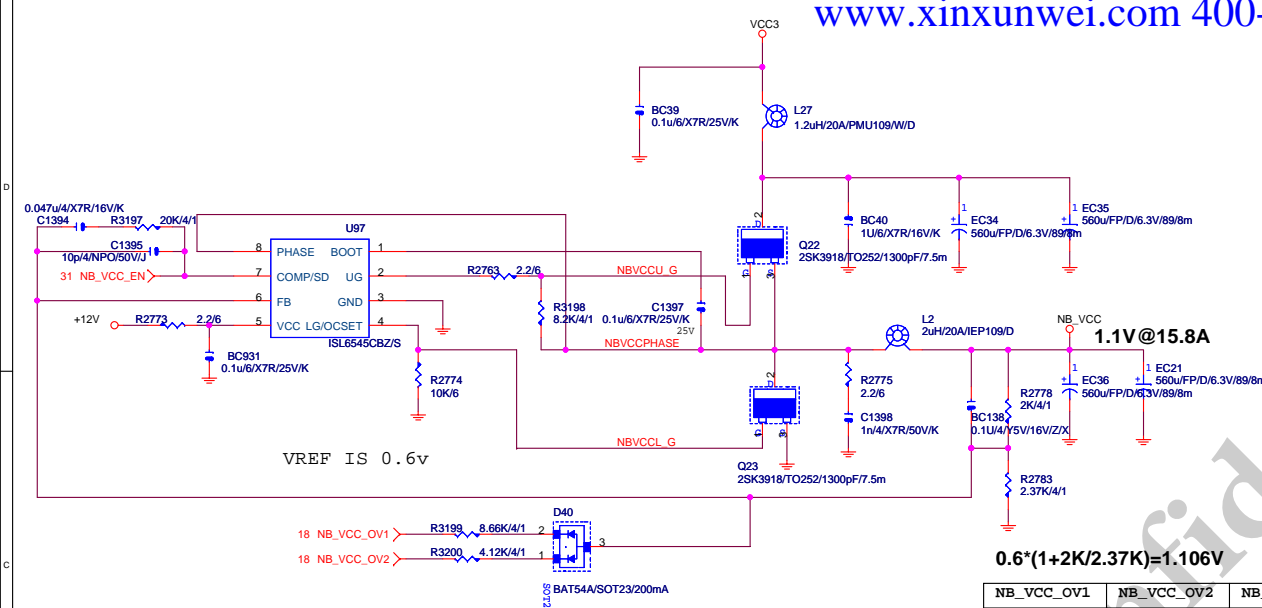
PWOK > NB_PWROK / SB_PWROK

15,29 RESET

17,27,33 -SLP_S3

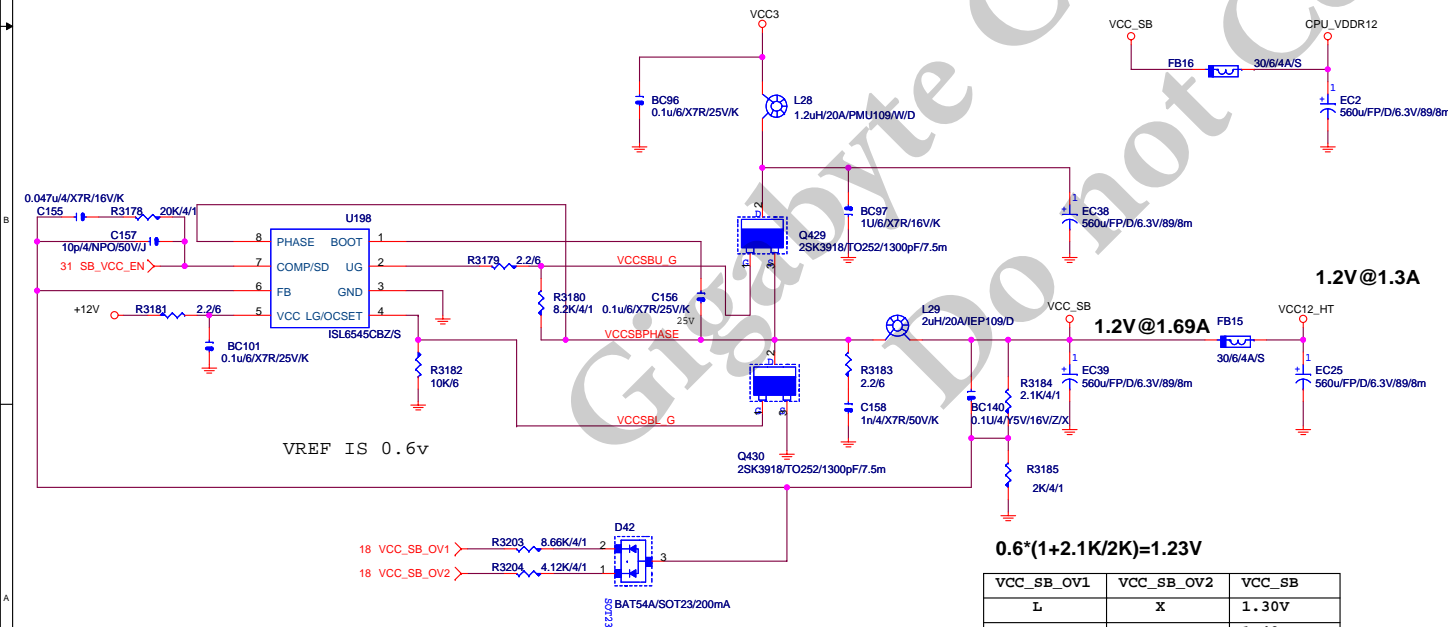
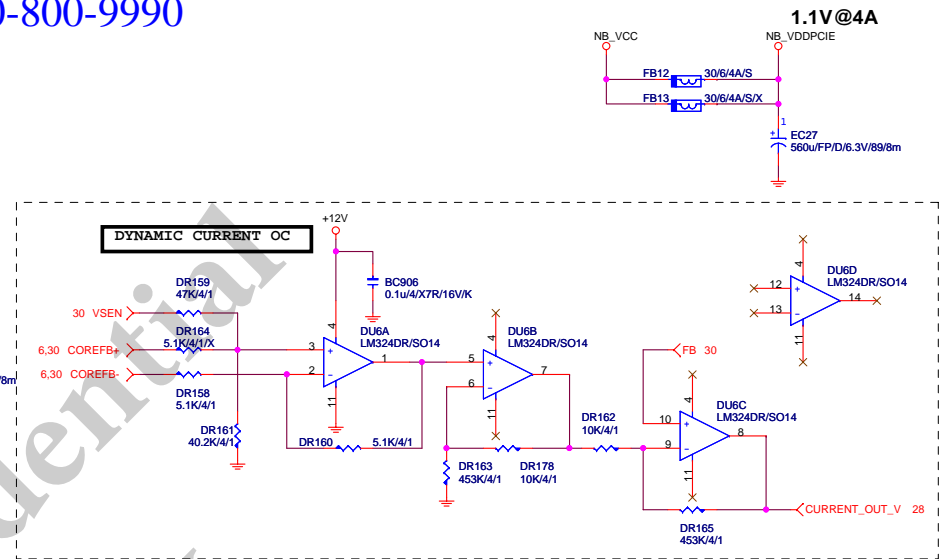
For ACC Function

D46 BAT154A/SOT23/200mA



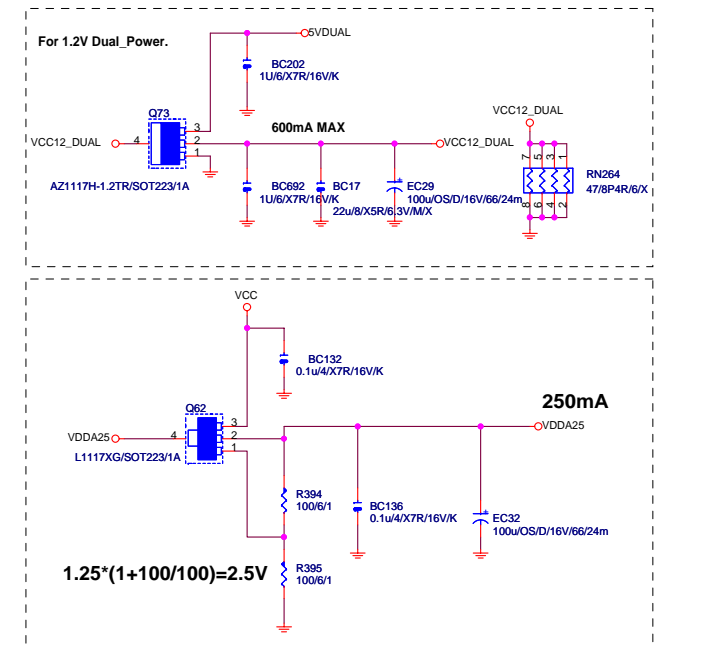
$$0.6 \times (1 + 2K/2.37K) = 1.106V$$

NB_VCC_OV1	NB_VCC_OV2	NB_VCC
L	X	1.20V
X	L	1.30V
L	L	1.40V

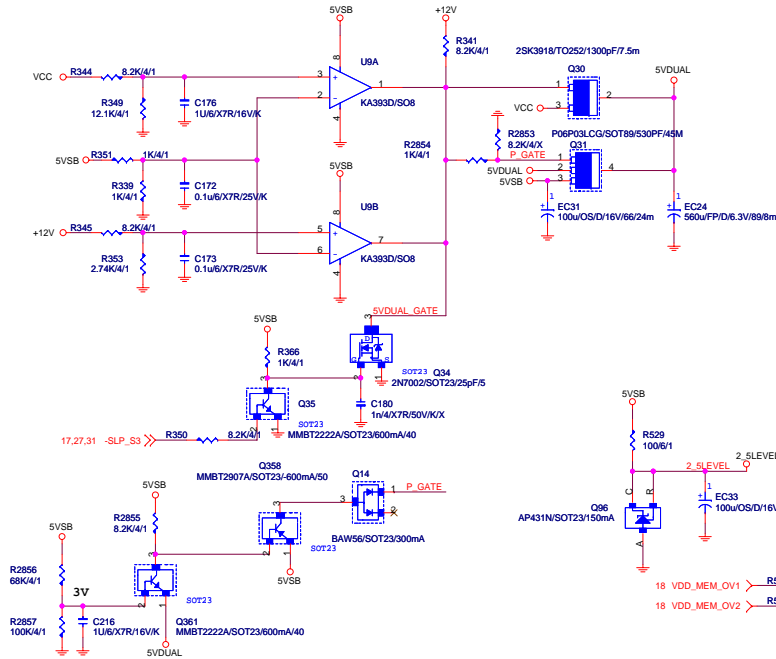


$$0.6 \times (1 + 2.1K/2K) = 1.23V$$

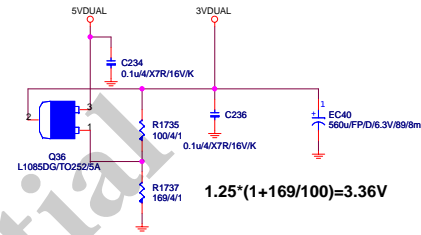
VCC_SB_OV1	VCC_SB_OV2	VCC_SB
L	X	1.30V
X	L	1.40V
L	L	1.50V



5VDUAL

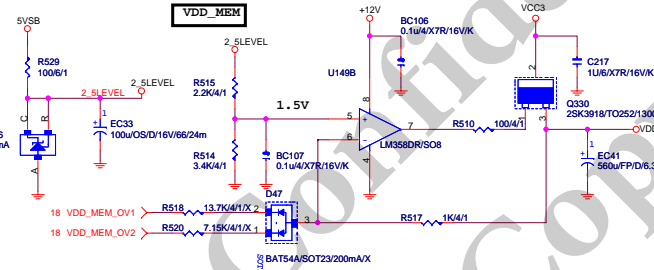


3VDUAL

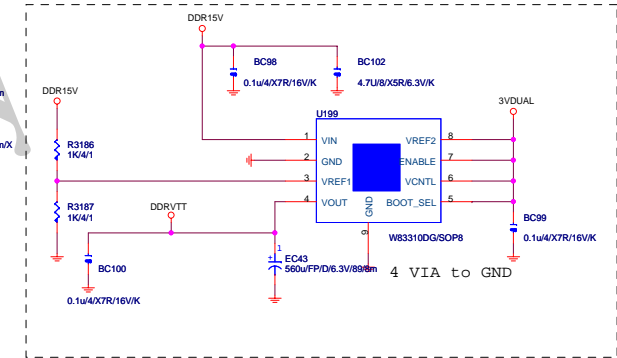


$$1.25 \times (1 + 169/100) = 3.36V$$

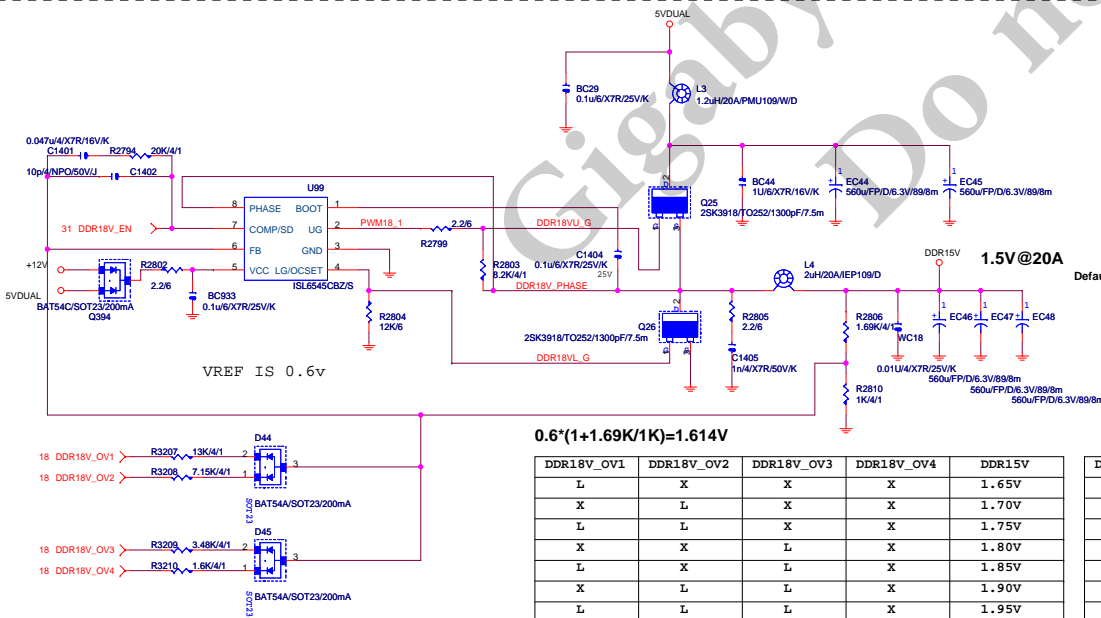
VDD_MEM



VDD_MEM_OV1	VDD_MEM_OV2	VDD_MEM
L	X	1.60V
X	L	1.70V
L	L	1.80V



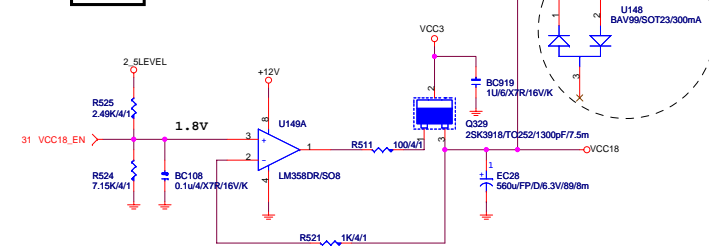
4 VIA to GND



$$0.6 \times (1 + 1.69K/1K) = 1.614V$$

DDR18V_OV1	DDR18V_OV2	DDR18V_OV3	DDR18V_OV4	DDR15V
L	X	X	X	1.65V
X	L	X	X	1.70V
L	L	X	X	1.75V
X	X	L	X	1.80V
L	X	L	X	1.85V
X	L	L	X	1.90V
L	L	L	X	1.95V

VCC18



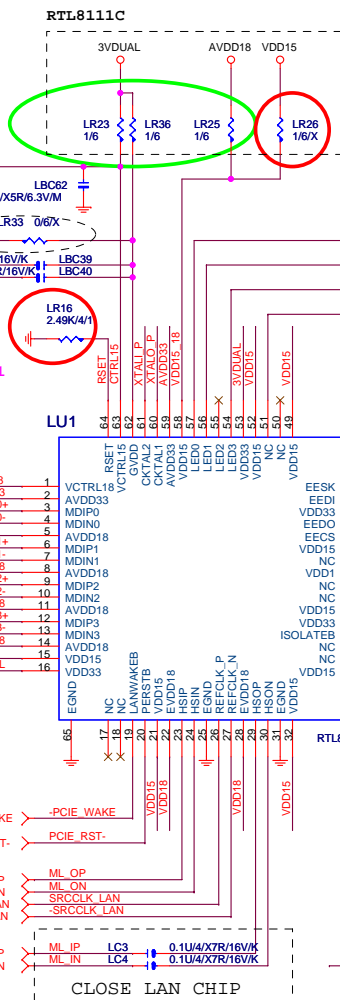
ATI for vcc3/vcc18 power ramp-up 2.1V

DDR18V_OV1	DDR18V_OV2	DDR18V_OV3	DDR18V_OV4	DDR15V
X	X	X	L	2.00V
L	X	X	L	2.05V
X	L	X	L	2.10V
L	L	X	L	2.15V
X	X	L	L	2.20V
L	X	L	L	2.25V
X	L	L	L	2.30V
L	L	L	L	2.35V

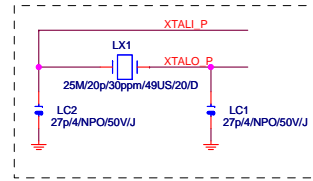
PCIE-1G LAN

LR33:0/6 DISABLE SWITCHING REG

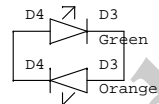
LR16:
RTL8101E-->2K/4/1
RTL8111C/8102E-->2.49K/4/1



LR36:
RTL8101E/8102E -->X
RTL8111C-->O



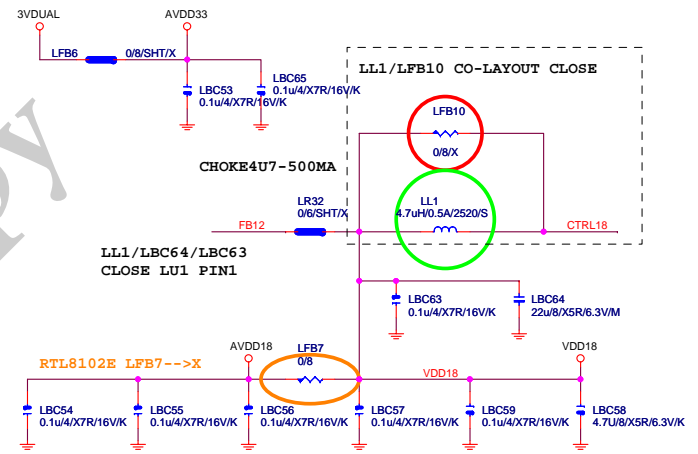
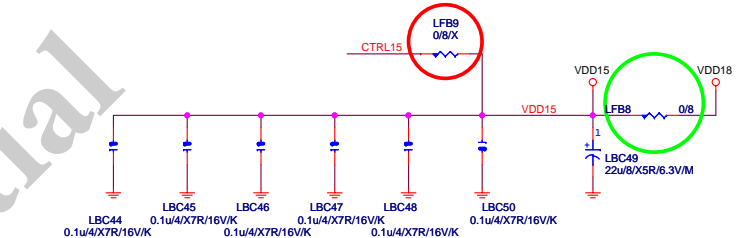
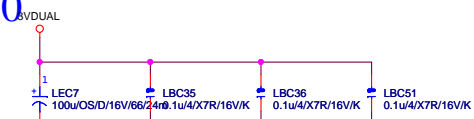
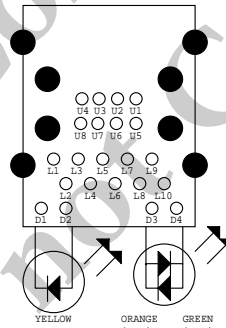
Dual Color LED



Single Color LED

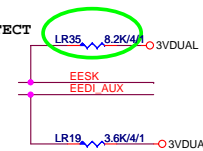


P35-152-19W9



FOR 93C46 OR BIOS DETECT

RTL8102E -->X

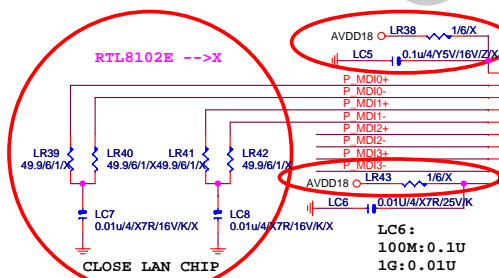


USB_LAN CONNECTOR

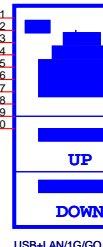
RTL8101E:LR38/LC5/LR43/LC6-->O
RTL8102E:LC5/LC6-->O
RTL8111C:LC6-->O

RTL8101E :L1+L10-->AVDD18+0.1U(BIOS DISABLE MDI-X FUNCTION)

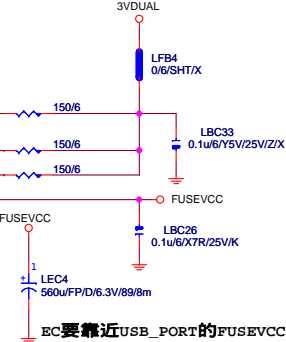
1G :USB+LAN/1G/GO,Y/OS/RA/D/1
100M:USB+LAN/100/GO,Y/OS/RA/D/1



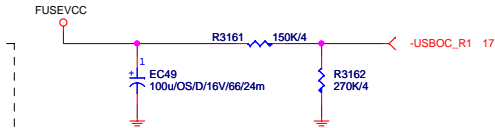
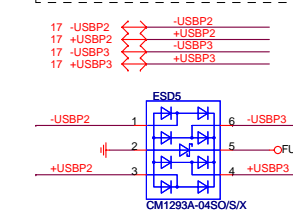
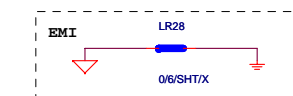
USB_LAN



USB+LAN/1G/GO,Y/OS/RA/D/1



USB_LAN



GIGABYTE

REALTK RTL8111C/8101E

GA-MA785GMT-UD2H

1.01

Date: Wednesday, June 17, 2009 Sheet 34 of 35

